University syllabus

Module-1

Diode Circuits: Review of diodes as rectifiers (No question shall be set from review portion). Diode clipping and clamping circuits.

Transistor biasing and stabilization: Operating point, analysis and design of fixed bias circuit, self-bias circuit, Emitter stabilized bias circuit, voltage divider bias circuit, stability factor of different biasing circuits. Problems.

Transistor switching circuits: Transistor switching circuits, PNP transistors, thermal compensation techniques.

Module-2

Transistor at low frequencies: BJT transistor modelling, CE fixed bias configuration, voltage divider bias, emitter follower, CB configuration, collector feedback configuration, analysis using h – parameter model, relation between h – parameters model of CE, CC and CB modes, Millers theorem and its dual.

Transistor frequency response: General frequency considerations, low frequency response, Miller effect capacitance, high frequency response, multistage frequency effects.

Module-3

Multistage amplifiers: Cascade and cascode connections, Darlington circuits, analysis and design.

Feedback amplifiers: Feedback concept, different types, practical feedback circuits, analysis and design of feedback circuits.

Module-4

Power amplifiers: Amplifier types, analysis and design of different power amplifiers, distortion in power amplifiers.

Oscillators: Principle of operation, analysis and derivation of frequency of oscillation of phase shift oscillator, Wien bridge oscillator, RF and crystal oscillator and frequency stability.

Module-5

FETs: Construction, working and characteristics of JFET and MOSFET. Biasing of JFET and MOSFET, JFET and MOSFET amplifiers, analysis and design.

Table of Contents

Module-1

Diode circuits

Diode:

A pure silicon crystal or germanium crystal is known as an intrinsic semiconductor. There are not enough free electrons and holes in an intrinsic semi-conductor to produce a usable current. The electrical action of these can be modified by doping means adding impurity atoms to a crystal to increase either the number of free holes or no of free electrons.

When a crystal has been doped, it is called a extrinsic semi-conductor. They are of two types

- n-type semiconductor having free electrons as majority carriers
- p-type semiconductor having free holes as majority carriers

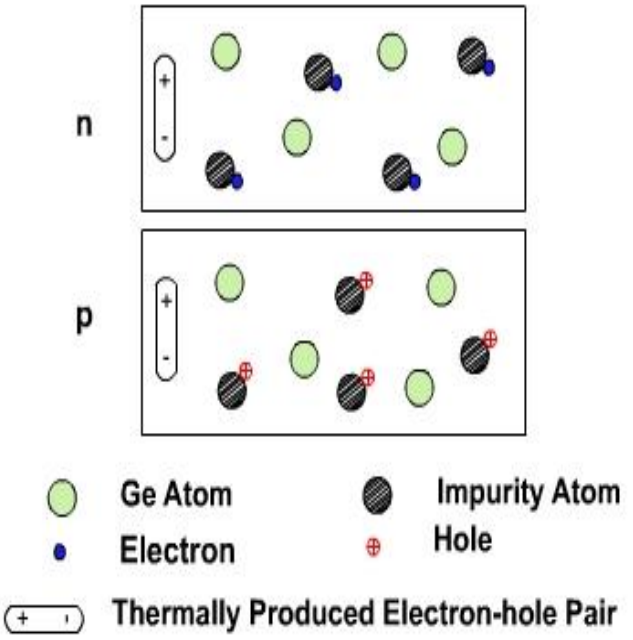
By themselves, these doped materials are of little use. However, if a junction is made by joining p-type semiconductor to n-type semiconductor a useful device is produced known as diode. It will allow current to flow through it only in one direction. The unidirectional properties of a diode allow current flow when forward biased and disallow current flow when reversed biased. This is called rectification process and therefore it is also called rectifier.

How is it possible that by properly joining two semiconductors each of which, by itself, will freely conduct the current in any direct refuses to allow conduction in one direction.

Consider first the condition of p-type and n-type germanium just prior to joining **fig. 1**. The majority and minority carriers are in constant motion.

The minority carriers are thermally produced and they exist only for short time after which they recombine and neutralize each other. In the mean time, other minority carriers have been produced and this process goes on and on.

The number of these electron hole pair that exist at any one time depends upon the temperature. The number of majority carriers is however, fixed depending on the number of impurity atoms available. While the electrons and holes are in motion but the atoms are fixed in place and do not move.



- Holes from the p-side diffuse into n-side where they recombine with free electrons.
- Free electrons from n-side diffuse into p-side where they recombine with free holes.
- The diffusion of electrons and holes is due to the fact that large no of electrons are concentrated in one area and large no of holes are concentrated in another area.
- When these electrons and holes begin to diffuse across the junction then they collide each other and negative charge in the electrons cancels the positive charge of the hole and both will lose their charges.
- The diffusion of holes and electrons is an electric current referred to as a recombination current. The recombination process decay exponentially with both time and distance from the junction. Thus most of the recombination occurs just after the junction is made and very near to junction.
- A measure of the rate of recombination is the lifetime defined as the time required for the density of carriers to decrease to 37% to the original concentration
- The impurity atoms are fixed in their individual places. The atoms itself is a part of the crystal and so cannot move. When the electrons and hole meet, their individual charge is cancelled and this leaves the originating impurity atoms with a net charge, the atom that produced the electron now lack an electronic and so becomes charged positively, whereas the atoms that produced the hole now lacks a positive charge and becomes negative.
- The electrically charged atoms are called ions since they are no longer neutral. These ions produce an electric field as shown in **fig. 3**. After several collisions occur, the electric field is great enough to repel rest of the majority carriers away of the junction. For example, an electron trying to diffuse from n to p side is repelled by the negative charge of the p-side. Thus diffusion process does not continue indefinitely but continues as long as the field is developed.
- This region is produced immediately surrounding the junction that has no majority carriers. The majority carriers have been repelled away from the junction and junction is depleted from

carriers. The junction is known as the barrier region or depletion region. The electric field represents a potential difference across the junction also called ***space charge potential or barrier potential .*** This potential is 0.7v for Si at 25^{o} celcious and 0.3v for Ge.

- The physical width of the depletion region depends on the doping level. If very heavy doping is used, the depletion region is physically thin because diffusion charge need not travel far across the junction before recombination takes place (short life time). If doping is light, then depletion is more wide (long life time).

The symbol of diode is shown in **fig. 4**. The terminal connected to p-layer is called anode (A) and the terminal connected to n-layer is called cathode (K)

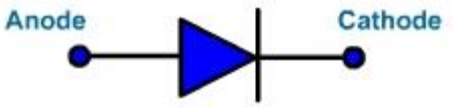
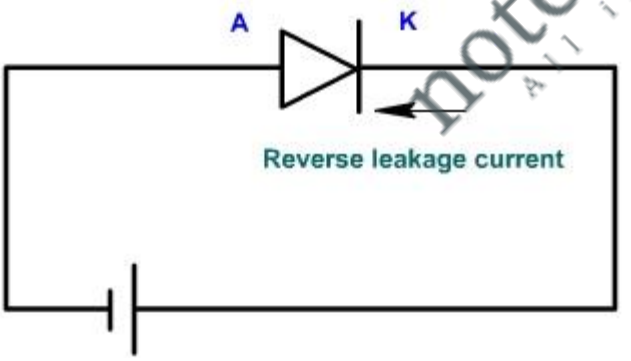


Fig.4

Reverse Bias:

If positive terminal of dc source is connected to cathode and negative terminal is connected to anode, the diode is called reverse biased as shown in **fig. 5**.



Space charge capacitance C_T of diode:

Reverse bias causes majority carriers to move away from the junction, thereby creating

more ions. Hence the thickness of depletion region increases. This region behaves as the dielectric material used for making capacitors. The p-type and n-type conducting on each side of dielectric act as the plate. The incremental capacitance C_T is defined by

$$C_T = \left|\frac{dQ}{dV}\right|$$

Since $i = \frac{dQ}{dt}$

Therefore, $i = C_T \frac{dV}{dt}$ **(E-1)**

where, dQ is the increase in charge caused by a change dV in voltage. C_T is not constant, it depends upon applied voltage, there fore it is defined as dQ / dV.

When p-n junction is forward biased, then also a capacitance is defined called *diffusion capacitance* C_D (rate of change of injected charge with voltage) to take into account the time delay in moving the charges across the junction by the diffusion process. It is considered as a fictitious element that allow us to predict time delay.

If the amount of charge to be moved across the junction is increased, the time delay is greater, it follows that diffusion capacitance varies directly with the magnitude of forward current.

$$C_D = \frac{dQ}{dV} = \frac{I\tau}{dV} \quad \textbf{(E-2)}$$

Relationship between Diode Current and Diode Voltage

An exponential relationship exists between the carrier density and applied potential of diode junction as given in equation E-3. This exponential relationship of the current i_D and the voltage v_D holds over a range of at least seven orders of magnitudes of current - that is a factor of 10^7.

$$i_D = I_0 \left[\exp\left(\frac{qv_D}{nkT} \right) - 1 \right] = I_0 \left[e^{\left(\frac{qv_D}{nkT} \right)} - 1 \right] \quad \textbf{(E-3)}$$

Where,

i_D= Current through the diode (dependent variable in this expression)
v_D= Potential difference across the diode terminals (independent variable in this expression)
I_O= Reverse saturation current (of the order of 10^{-15} A for small signal diodes, but I_O is a

strong function of temperature)
q = Electron charge: 1.60 x 10^{-19} joules/volt
k = Boltzmann's constant: 1.38 x $l0^{-23}$ joules /° K
T = Absolute temperature in degrees Kelvin (°K = 273 + temperature in °C)
n = Empirical scaling constant between 0.5 and 2, sometimes referred to as the Exponential Ideality Factor

The empirical constant, n, is a number that can vary according to the voltage and current levels. It depends on electron drift, diffusion, and carrier recombination in the depletion region. Among the quantities affecting the value of n are the diode manufacture, levels of doping and purity of materials. If n=1, the value of k T/ q is 26 mV at 25°C. When n=2, k T/ q becomes 52 mV.

For germanium diodes, n is usually considered to be close to 1. For silicon diodes, n is in the range of 1.3 to 1.6. n is assumed 1 for all junctions all throughout unless otherwise noted.

Equation **(E-3)** can be simplified by defining V_T =k T/q, yielding

$$i_D = I_O\left[\exp\left(\frac{v_D}{nV_T}\right) - 1\right] = I_O\left[e^{\left(\frac{v_D}{nV_T}\right)} - 1\right] \qquad \textbf{(E-4)}$$

At room temperature (25°C) with forward-bias voltage only the first term in the parentheses is dominant and the current is approximately given by

$$i_D = I_O\, e^{\frac{v_D}{nV_T}} \qquad \textbf{(E-5)}$$

The current-voltage (l-V) characteristic of the diode, as defined by (E-3) is illustrated in **fig. 1**. The curve in the figure consists of two exponential curves. However, the exponent values are such that for voltages and currents experienced in practical circuits, the curve sections are close to being straight lines. For voltages less than V_{ON}, the curve is approximated by a straight line of slope close to zero. Since the slope is the conductance (i.e., i / v), the conductance is very small in this region, and the equivalent resistance is very high. For voltages above V_{ON}, the curve is approximated by a straight line with a very large slope. The conductance is therefore very large, and the diode has a very small equivalent resistance.

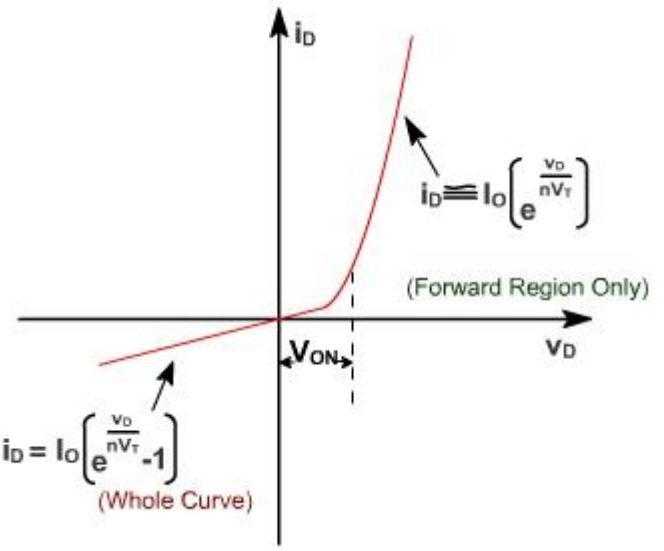


Fig.1 - Diode Voltage relationship

The slope of the curves of **fig.1** changes as the current and voltage change since the l-V characteristic follows the exponential relationship of relationship of equation (E-4). Differentiate the equation (E-4) to find the slope at any arbitrary value of $v_D$or i_D,

$$\frac{di_D}{dv_D} = \frac{I_O}{nV_T}\exp\left(\frac{v_D}{nV_T}\right) = \frac{I_O}{nV_T}e^{\frac{v_D}{nV_T}} \qquad \textbf{(E-6)}$$

This slope is the equivalent conductance of the diode at the specified values of v_D or i_D.

We can approximate the slope as a linear function of the diode current. To eliminate the exponential function, we substitute equation (E-4) into the exponential of equation (E-7) to obtain

$$\exp\left(\frac{v_D}{nV_T}\right) = \frac{i_D}{I_O} + 1 = \left(\frac{di_D}{dv_D}\right)\left(\frac{nV_T}{i_D}\right) \qquad \textbf{(E-7)}$$

A realistic assumption is that $I_O << i_D$ equation (E-7) then yields,

$$\frac{di_D}{dv_D} = \frac{i_D + I_O}{nV_T} \approx \frac{i_D}{nV_T} \qquad \textbf{(E-8)}$$

The approximation applies if the diode is forward biased. The dynamic resistance is the reciprocal of this expression.

$$r_d = \frac{nV_T}{i_D + I_0} \approx \frac{nV_T}{i_D} \qquad \textbf{(E-9)}$$

Although r_d is a function of i_d, we can approximate it as a constant if the variation of i_D is small. This corresponds to approximating the exponential function as a straight line within a specific operating range.

Normally, the term R_f to denote diode forward resistance. R_f is composed of r_d and the contact resistance. The contact resistance is a relatively small resistance composed of the resistance of the actual connection to the diode and the resistance of the semiconductor prior to the junction. The reverse-bias resistance is extremely large and is often approximated as infinity.

Temperature Effects:

Temperature plays an important role in determining the characteristic of diodes. As temperature increases, the turn-on voltage, v_{ON}, decreases. Alternatively, a decrease in temperature results in an increase in v_{ON}. This is illustrated in **fig. 2,** where V_{ON} varies linearly with temperature which is evidenced by the evenly spaced curves for increasing temperature in 25 °C increments.

The temperature relationship is described by equation

$$V_{ON}(T_{New}) - V_{ON}(T_{room}) = k_T(T_{New} - T_{room}) \qquad \textbf{(E-10)}$$

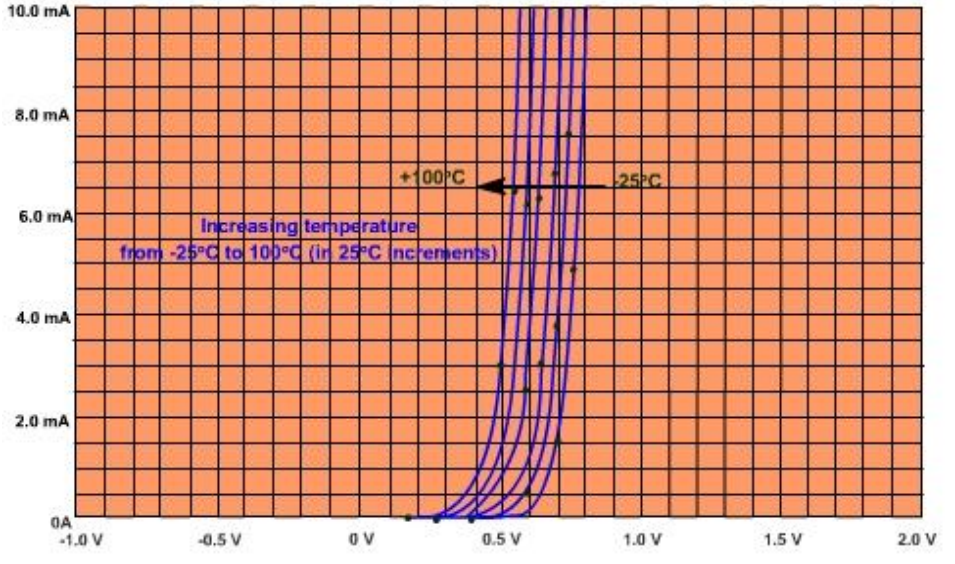


Fig. 2 - Dependence of iD on temperature versus vD for real diode (kT = -2.0 mV /°C)

where,

T_{room}= room temperature, or 25°C.
T_{New}= new temperature of diode in °C.
$V_{ON}(T_{room})$ = diode voltage at room temperature.
$V_{ON}(T_{New})$ = diode voltage at new temperature.
k_T = temperature coefficient in V/°C.

Although k_T varies with changing operating parameters, standard engineering practice permits approximation as a constant. Values of k_T for the various types of diodes at room temperature are given as follows:

k_T= -2.5 mV/°C for germanium diodes
k_T = -2.0 mV/°C for silicon diodes

The reverse saturation current, I_O also depends on temperature. At room temperature, it increases approximately 16% per °C for silicon and 10% per °C for germanium diodes. In other words, I_O approximately doubles for every 5 °C increase in temperature for silicon, and for every 7 °C for germanium. The expression for the reverse saturation current as a function of temperature can be approximated as

$$I_0(atT_2) = I_0(atT_1)\exp(k_i(T_2 - T_1)) = I_0(atT_1)e^{K_i(T_2 - T_1)} \quad \textbf{(E-11)}$$

where K_i= 0.15/°C (for silicon) and T1 and T2 are two arbitrary temperatures.

Diode Operating Point

Example - 1:

When a silicon diode is conducting at a temperature of 25°C, a 0.7 V drop exists across its terminals. What is the voltage, V_{ON}, across the diode at 100°C?

Solution:

The temperature relationship is described by

$V_{ON}(T_{New}) - V_{ON}(T_{room}) = K_T (T_{New} - T_{room})$

or, $V_{ON}(T_{New}) = V_{ON}(T_{room}) + K_T (T_{new} - T_{room})$

Given $V_{ON}(T_{room}) = 0{,}7$ V, T_{room}= 25° C, T_{New}= 100° C

Therefore, $V_{ON}(T_{New}) = 0.7 + (-2 \times 10^{-3})(100-75) = 0.55$ V

Example - 2:

Find the output current for the circuit shown in **fig.1(a).**

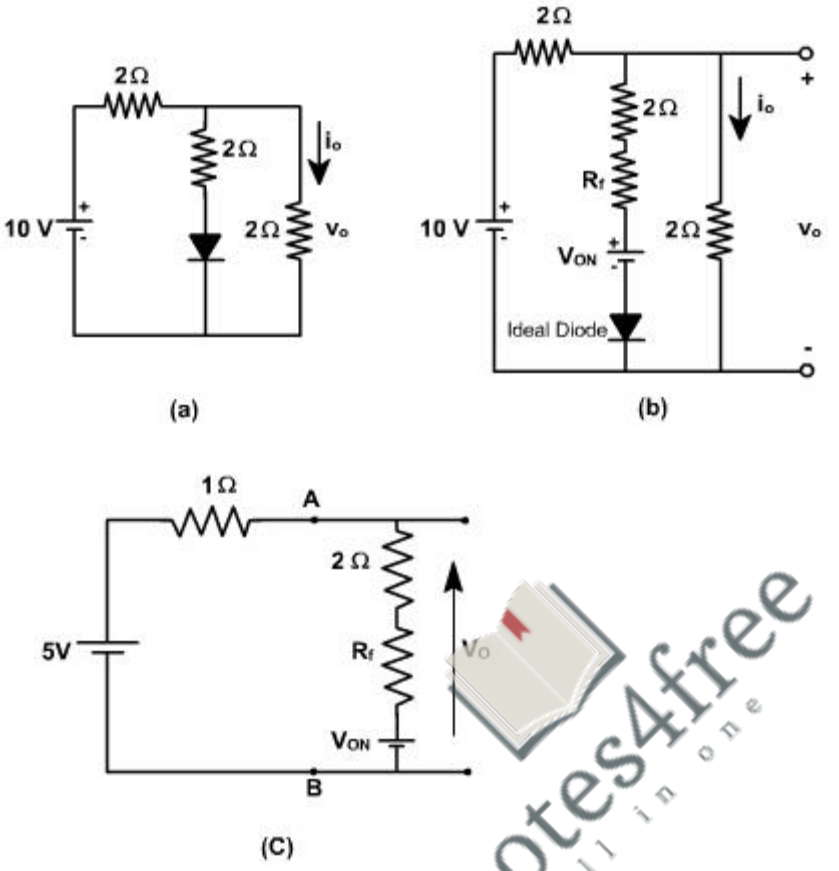


Fig.1- Circuit for Example 2

Solutions:

Since the problem contains only a dc source, we use the diode equivalent circuit, as shown in **fig. 1(b).** Once we determine the state of the ideal diode in this model (i.e., either open circuit or short circuit), the problem becomes one of simple dc circuit analysis.

It is reasonable to assume that the diode is forward biased. This is true since the only external source is 10 V, which clearly exceeds the turn-on voltage of the diode, even taking the voltage division into account. The equivalent circuit then becomes that of **fig. 1(b).** with the diode replaced by a short circuit.

The Thevenin's equivalent of the circuit between A and B is given by **fig. 1(c).**

The output voltage is given by

$$v_o = \left(\frac{5 - V_{ON}}{3 + R_f}\right)(2 + R_f) + V_{ON}$$

or, $$v_o = \frac{10 + V_{ON} + 5R_f}{3 + R_f}$$

If V_{ON}= 0.7V, and R_f= 0.2 W , then

V_o = 3.66V

Diode Operating Point

Example - 3

The circuit of fig. 2, has a source voltage of Vs = 1.1 + 0.1 sin 1000t. Find the current, iD. Assume that

nVT = 40 mV

VON = 0.7 V

Solution:

We use KVL for dc equation to yield

$V_s = V_{ON} + I_D R_L$

$$I_D = \frac{V_S - V_{ON}}{R_L} = 4 \text{ mA}$$

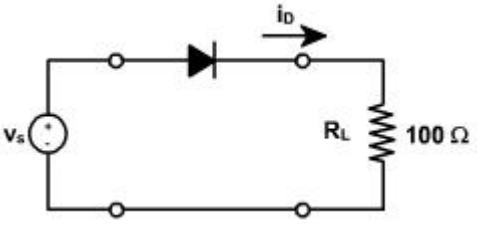


Fig.2

This sets the dc operating point of the diode. We need to determine the dynamic resistance so we can establish the resistance of the forward-biased junction for the ac signal.

$$r_D = \frac{nV_T}{I_D} = 10\ \Omega$$

Assuming that the contact resistance is negligible Rf= rD Now we can replace the forward-biased diode with a 10 W resistor. Again using KVL, we have,

vs= Rf id + RL id

$$i_d = \frac{v_S}{R_f + R_L} = 0.91 \sin 1000\,t \quad mA$$

The diode current is given by

I = 4 + 0.91 sin 1000 t mA

Since iD is always positive, the diode is always forward-biased, and the solution is complete.

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Diode Operating Point

Small Signal Operation of Real diode:

Consider the diode circuit shown in **fig. 3**.

$V = V_D + I_d R_L$

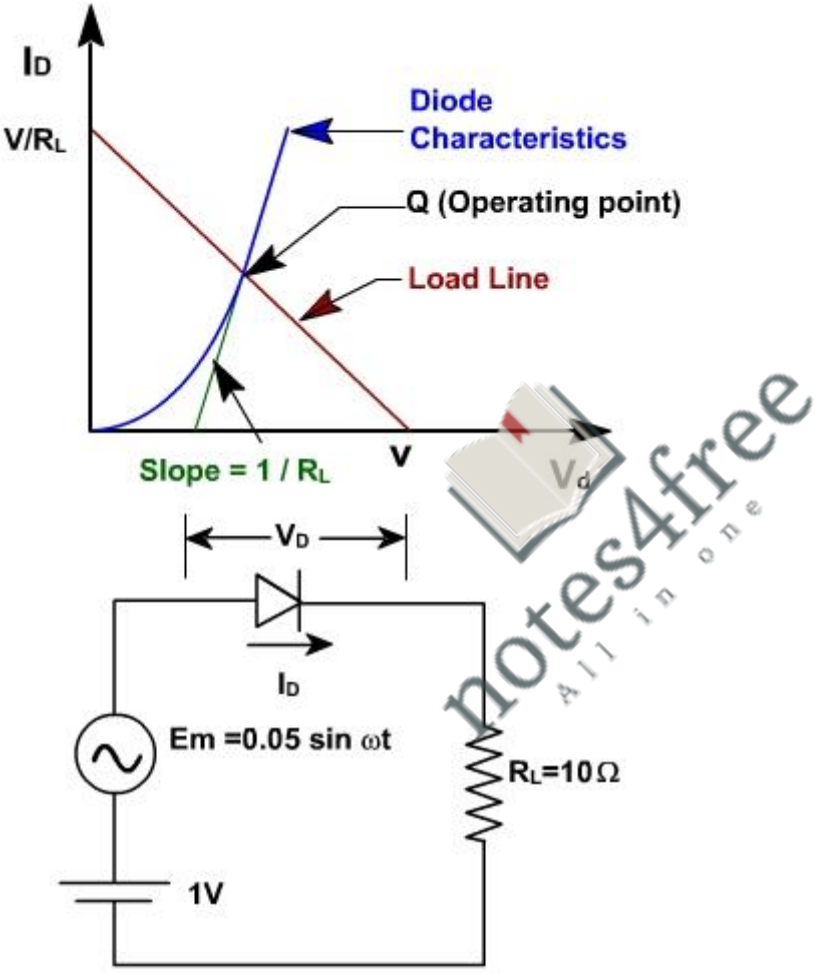
$V_D = V - I_d R_L$

This equation involves two unknowns and cannot be solved. The straight line represented by the above equation is known as the **load line**. The load line passes through two points,

$I = 0, V_D = V$

and $V_D = 0, I = V / R_L$.

The slope of this line is equal to 1/ RL. The other equation in terms of these two variables VD & Id, is given by the static characteristic. The point of intersection of straight line and diode characteristic gives the operating point as shown in fig. 4.



ohm.

The resulting input voltage is the sum of dc voltage and sinusoidal ac voltage. Therefore, as the diode voltage varies, diode current also varies, sinusoidally. The intersection of load line and diode characteristic for different input voltages gives the output voltage as shown in fig. 6.

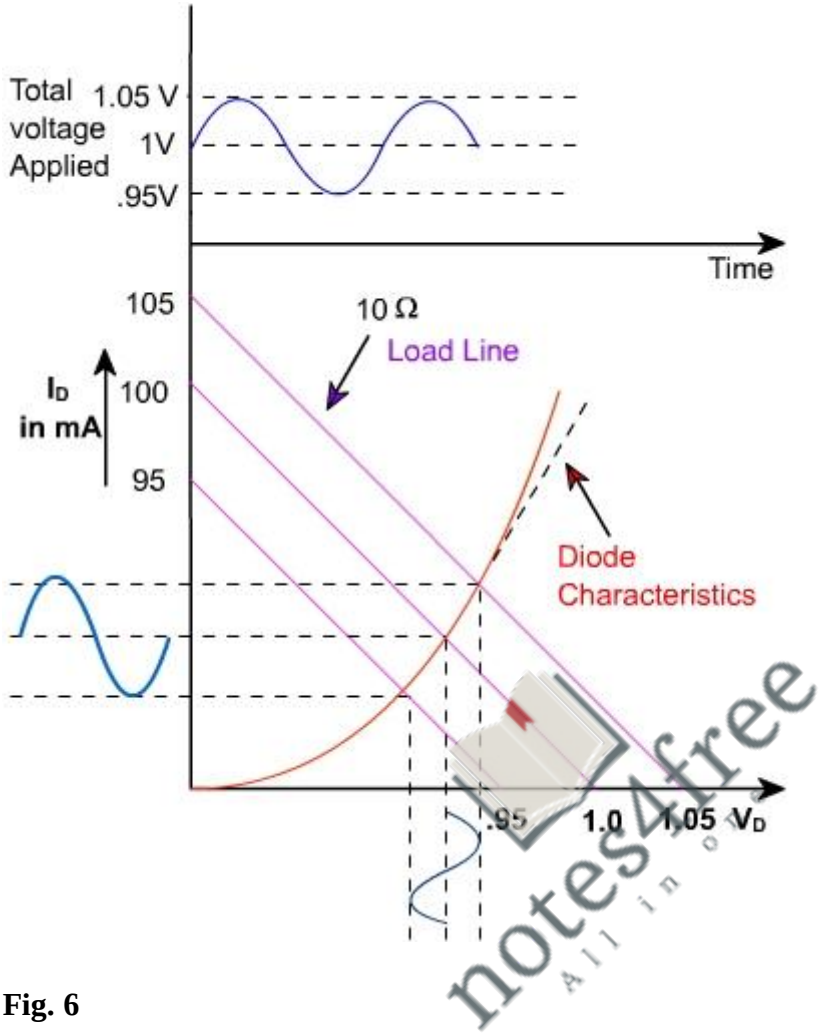
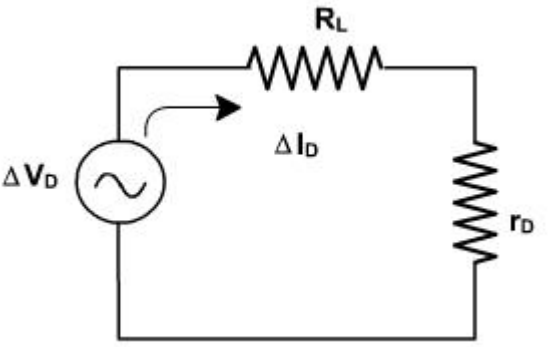


Fig. 6

In certain applications only ac equivalent circuit is required. Since only ac response of the circuit is considered DC Source is not shown in the equivalent circuit of fig. 7. The resistance rf represents the dynamic resistance or ac resistance of the diode. It is obtained by taking the ratio of Δ VD/ Δ ID at operating point.

Dynamic Resistance Δ rD = Δ VD / Δ ID

Let us consider a circuit shown in fig. 5 having dc voltage and sinusoidal ac voltage. Say



V = 1V, RL=10

Fig. 7

Applications of Diode

Diode Approximation: (Large signal operations):

1. Ideal Diode:

- **When diode is forward biased, resistance offered is zero,**
- **When it is reverse biased resistance offered is infinity. It acts as a perfect switch.**

The characteristic and the equivalent circuit of the diode is shown in fig. 1.

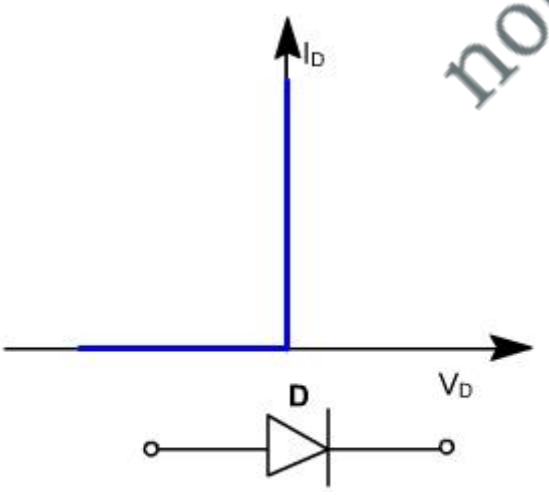


Fig. 1

2. Second Approximation:

- **When forward voltage is more than 0.7 V, for Si diode then it conducts and offers zero resistance. The drop across the diode is 0.7V.**
- **When reverse biased it offers infinite resistance.**

The characteristic and the equivalent circuit is shown in fig. 2.

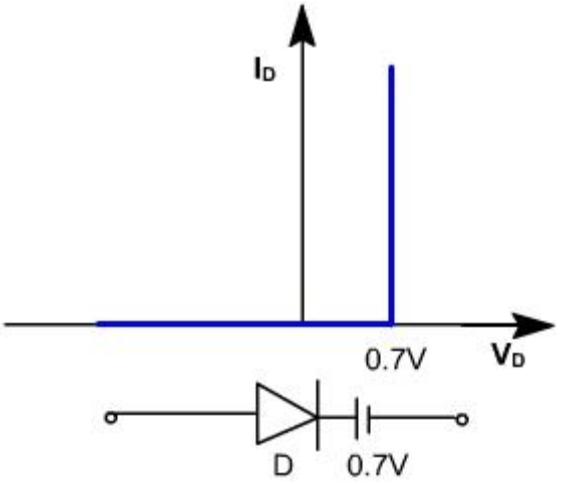


Fig. 2

3. 3rd Approximation:

- **When forward voltage is more than 0.7 V, then the diode conducts and the voltage drop across the diode becomes 0.7 V and it offers resistance Rf (slope of the current)**

VD= 0.7 + ID Rf.

The output characteristic and the equivalent circuit is shown in fig. 3.

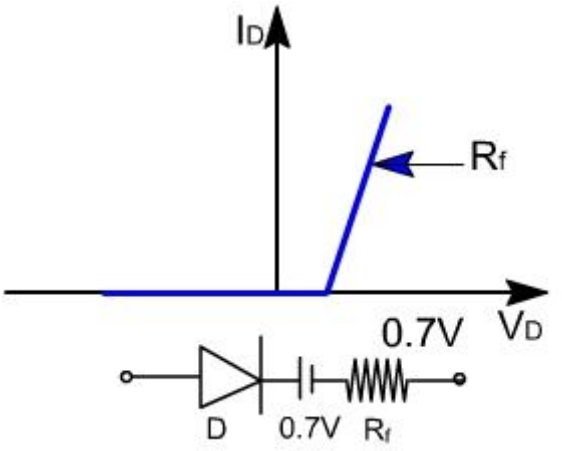


Fig. 3

- **When reverse biased resistance offered is very high & not infinity, then the diode equivalent circuit is as shown in fig. 4.**

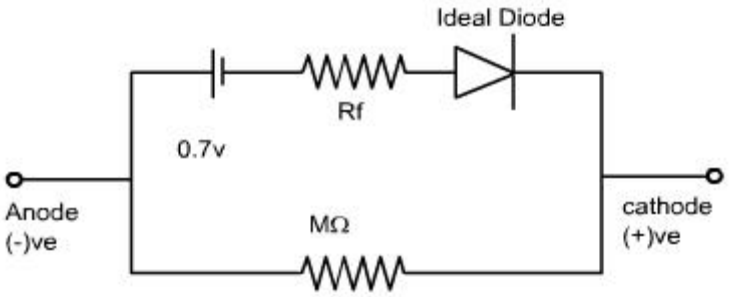


Fig. 4

Example - 1:

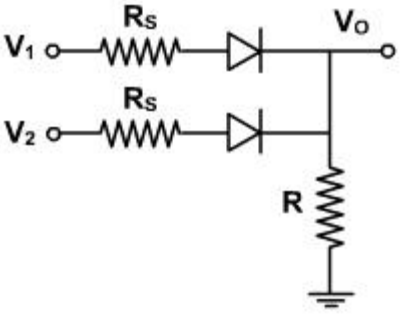
Calculate the voltage output of the circuit shown in **fig. 5** for following inputs

(a) $V_1 = V_2 = 0$.

(b) $V_1 = V$, $V_2 = 0$.

(c) $V_1 = V_2 = V$ knew voltage = V_r

Forward resistance of each diode is R_f.



Solution:

(a). When both V_1 and V_2 are zero , then the diodes are unbiased. Therefore,

$V_o = 0$ V

(b). When $V_1 = V$ and $V_2 = 0$, then one upper diode is forward biased and lower diode is unbiased. The resultant circuit using third approximation of diode will be as shown in **fig. 6**.

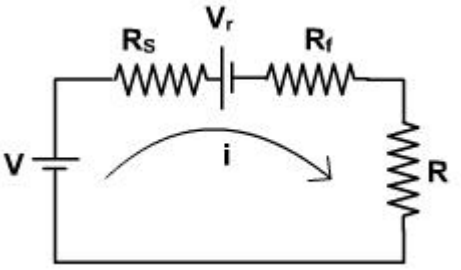


Fig. 6

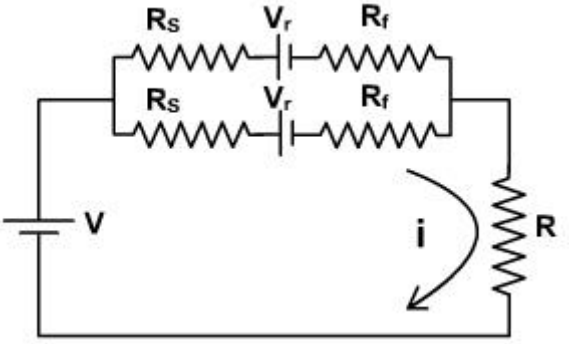


Fig. 7

Applying KVL, we get

$$V = I(R_f + R_s + R) + V_r$$

$$\therefore I = \frac{V - Vr}{R_s - R_f + R}$$

(c) When both V_1 and V_2 are same as V, then both the diodes are forward biased and conduct. The resultant circuit using third approximation of diode will be as shown in **Fig. 7**.

$$V = \frac{1}{2}(R_f + R_s) + V_r + 1$$

$$I = \frac{V - V_r}{\left(\frac{R_s + R_f}{2} + R\right)}$$

Half wave Rectifier:

The single ? phase half wave rectifier is shown in **fig. 8**.

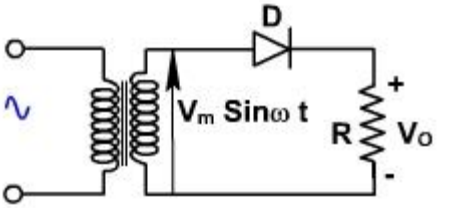


Fig. 8

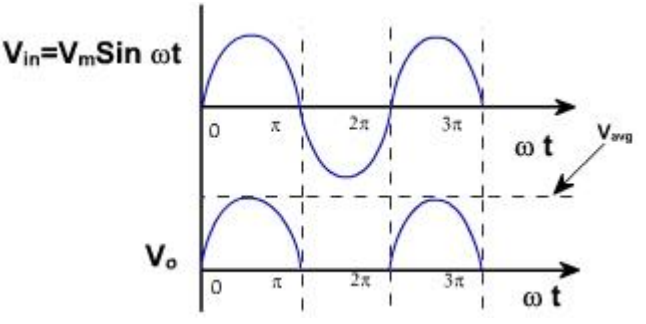


Fig. 9

In positive half cycle, D is forward biased and conducts. Thus the output voltage is same as the input voltage. In the negative half cycle, D is reverse biased, and therefore output voltage is zero. The output voltage waveform is shown in **fig. 9**.

The average output voltage of the rectifier is given by

$$V_{avg} = \frac{1}{2}\int_0^{\pi} V_m \sin \omega t \, d(\omega t)$$

$$= \frac{V_m}{\pi} = 0.318 V_m$$

The average output current is given by

$$I_{avg} = \frac{V_m}{\pi R}$$

When the diode is reverse biased, entire transformer voltage appears across the diode. The maximum voltage across the diode is V_m. The diode must be capable to withstand this voltage. Therefore PIV half wave rating of diode should be equal to V_m in case of single-phase rectifiers. The average current rating must be greater than I_{avg}

Full Wave Rectifier:

A single ? phase full wave rectifier using center tap transformer is shown in **fig. 10.** It supplies current in both half cycles of the input voltage.

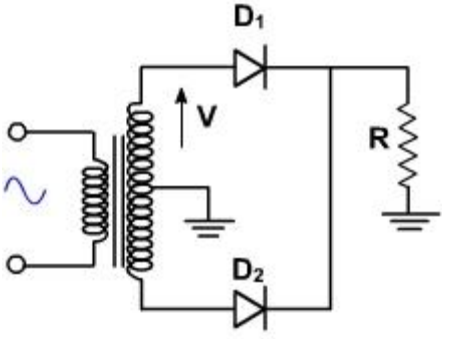


Fig. 10

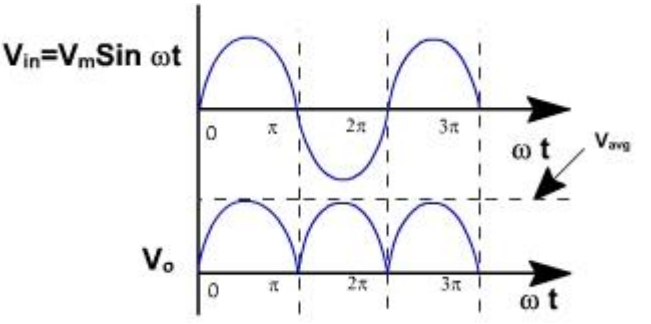


Fig. 11

In the first half cycle D_1 is forward biased and conducts. But D_2 is reverse biased and does not conduct. In the second half cycle D_2 is forward biased, and conducts and D_1 is reverse biased. It is also called 2 ? pulse midpoint converter because it supplies current in both the half cycles. The output voltage waveform is shown in **fig. 11**.

The average output voltage is given by

$$V_{avg} = \frac{1}{\pi}\int_0^{\pi} V_m \sin\omega t \, d(\omega t)$$
$$= \frac{2V_m}{\pi}$$

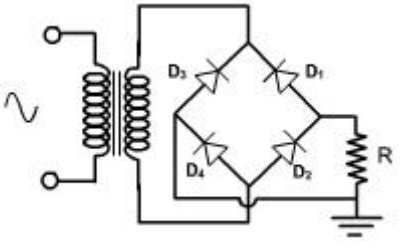
and the average load current is given by

$$I_{avg} = \frac{2V_m}{\pi R}$$

When D_1 conducts, then full secondary voltage appears across D_2, therefore PIV rating of the diode should be 2 V_m.

Bridge Rectifier:

The single ? phase full wave bridge rectifier is shown in **fig. 1.** It is the most widely used rectifier. It also provides currents in both the half cycle of input supply.



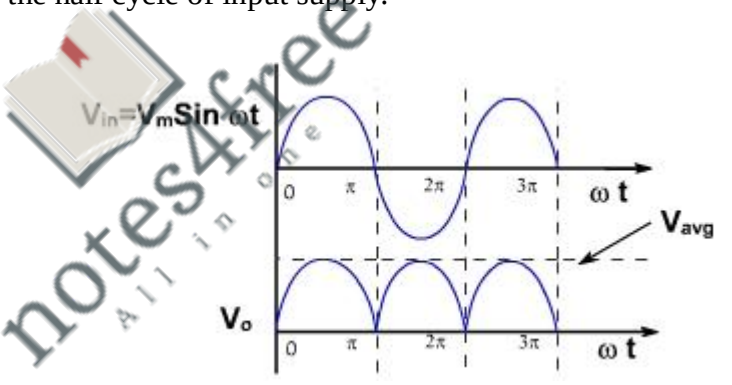


Fig. 1 **Fig. 2**

In the positive half cycle, D_1 & D_4 are forward biased and D_2 & D_3 are reverse biased. In the negative half cycle, D_2 & D_3 are forward biased, and D_1 & D_4 are reverse biased. The output voltage waveform is shown in **fig. 2** and it is same as full wave rectifier but the advantage is that PIV rating of diodes are V m and only single secondary transformer is required.

The main disadvantage is that it requires four diodes. When low dc voltage is required then secondary voltage is low and diodes drop (1.4V) becomes significant. For low dc output, 2-pulse center tap rectifier is used because only one diode drop is there.

The ripple factor is the measure of the purity of dc output of a rectifier and is defined as

$$\text{Ripple factor} = \frac{\text{r.m.s value of the ac output voltage}}{\text{average dc output voltage}}$$
$$= \sqrt{V_0^2 + \sum_{n=1}^{\infty} V_n^2}$$

Therefore,

$$\text{Ripple factor} = \frac{\sqrt{V_{rms}^2 - V_o^2}}{V_o}$$

$$= \sqrt{\left(\frac{V_{rms}}{V_o}\right)^2 - 1}$$

Clippers:

Clipping circuits are used to select that portion of the input wave which lies above or below some reference level. Some of the clipper circuits are discussed here. The transfer characteristic (v_o vs v_i) and the output voltage waveform for a given input voltage are also discussed.

Clipper Circuit 1:

The circuit shown in **fig. 3**, clips the input signal above a reference voltage (V_R).

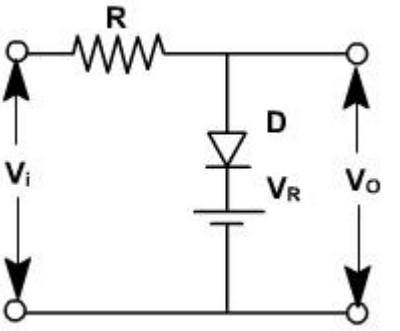


Fig. 3

In this clipper circuit,

If $v_i < V_R$, diode is reversed biased and does not conduct. Therefore, $v_o = v_i$

and, if $v_i > V_R$, diode is forward biased and thus, $v_o = V_R$.

The transfer characteristic of the clippers is shown in **fig. 4**.

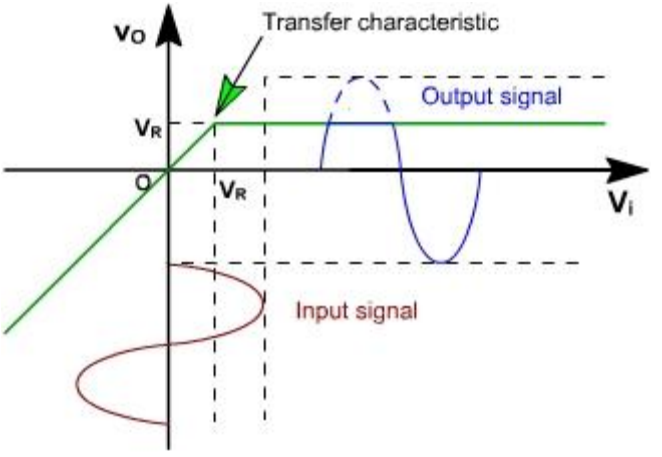


Fig. 4

Clipper Circuit 2:

The clipper circuit shown in **fig. 5** clips the input signal below reference voltage V_R.

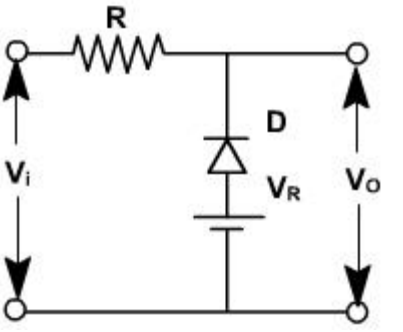


Fig. 5

In this clipper circuit,

If $v_i > V_R$, diode is reverse biased. $v_o = v_i$

and, If $v_i < V_R$, diode is forward biased. $v_o = V_R$

The transfer characteristic of the circuit is shown in **fig. 6**.

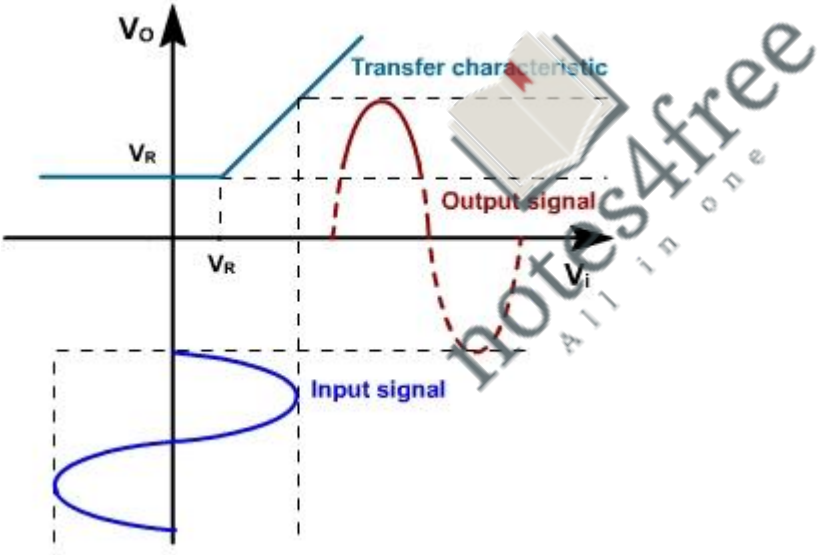


Fig. 6

Clipper Circuit 3: To clip the input signal between two independent levels ($V_{R1} < V_{R2}$), the clipper circuit is shown in **fig. 7**.

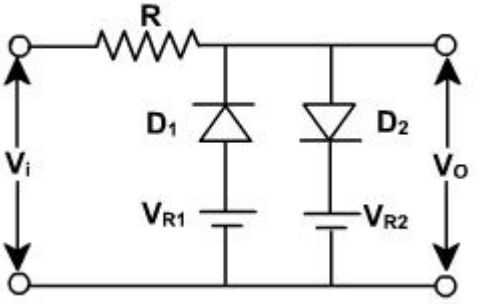


Fig. 7

The diodes D_1 & D_2 are assumed ideal diodes.

For this clipper circuit, when $v_i \leq V_{R1}$, $v_o = V_{R1}$

and, $v_i \geq V_{R2}$, $v_o = V_{R2}$

and, $V_{R1} < v_i < V_{R2}$ $v_o = v_i$

The transfer characteristic of the clipper is shown in **fig. 8.**

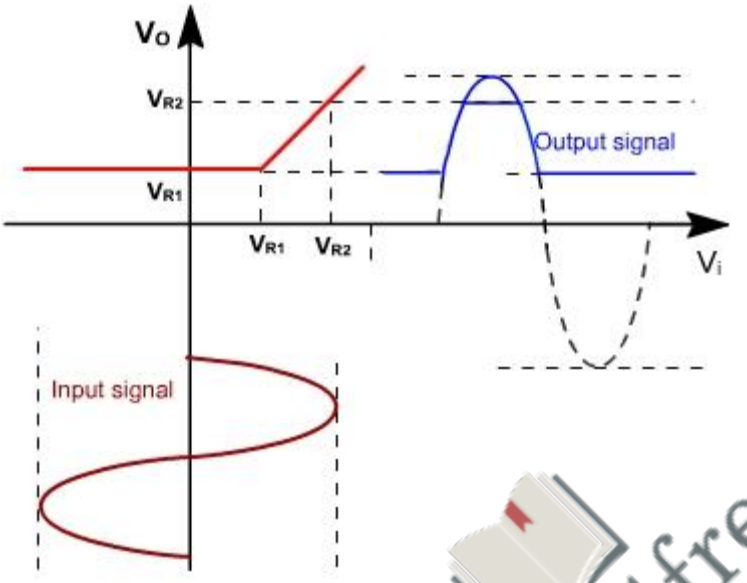


Fig. 8

Clippers:

Clipping circuits are used to select that portion of the input wave which lies above or below some reference level. Some of the clipper circuits are discussed here. The transfer characteristic (v_o vs v_i) and the output voltage waveform for a given input voltage are also discussed.

Clipper Circuit 1:

The circuit shown in **fig. 3**, clips the input signal above a reference voltage (V_R).

In this clipper circuit,

If $v_i < V_R$, diode is reversed biased and does not conduct. Therefore, $v_o = v_i$

and, if $v_i > V_R$, diode is forward biased and thus, $v_o = V_R$.

The transfer characteristic of the clippers is shown in **fig. 4.**

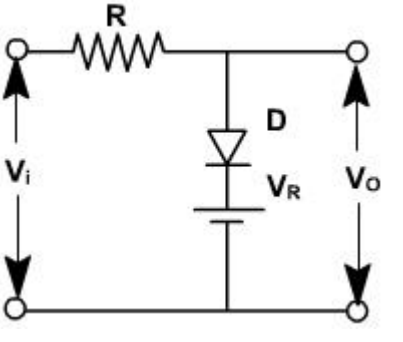


Fig. 3

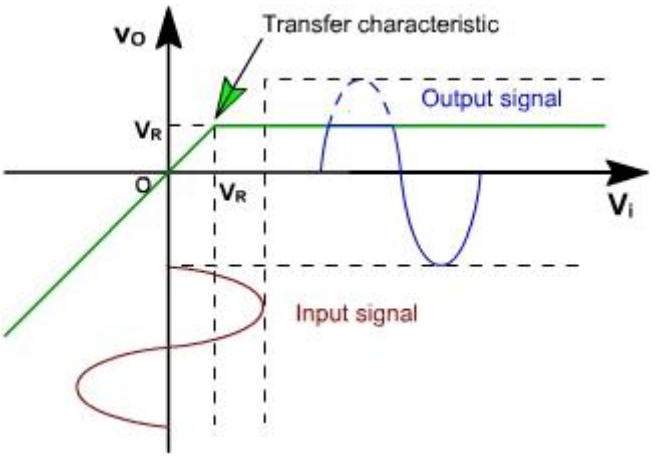


Fig. 4

Clipper Circuit 2:

The clipper circuit shown in **fig. 5** clips the input signal below reference voltage V_R.

In this clipper circuit,

If $v_i > V_R$, diode is reverse biased. $v_o = v_i$

and, If $v_i < V_R$, diode is forward biased. $v_o = V_R$

The transfer characteristic of the circuit is shown in **fig. 6**.

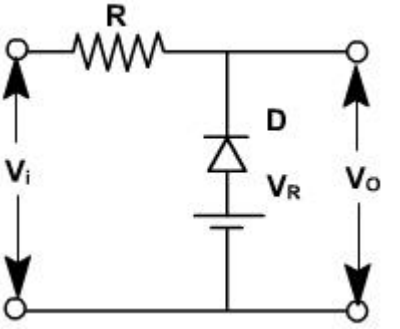


Fig. 5

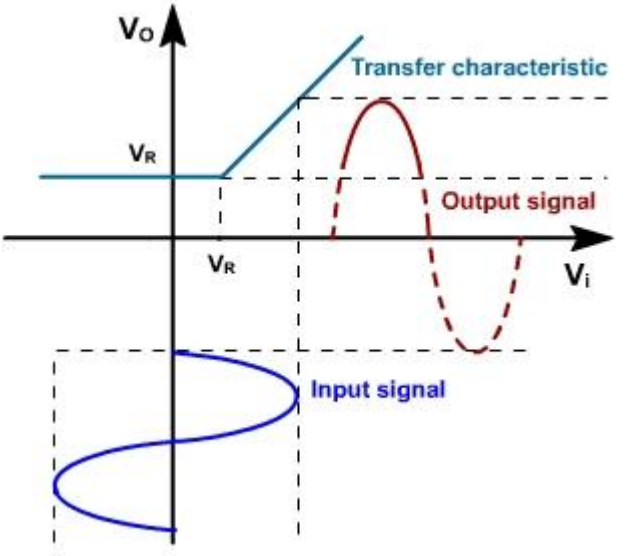


Fig. 6

Clipper Circuit 3:

To clip the input signal between two independent levels ($V_{R1} < V_{R2}$), the clipper circuit is shown in **fig. 7.**

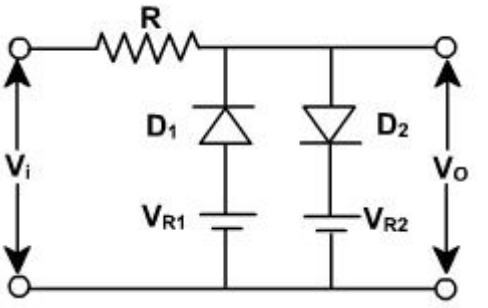


Fig. 7

The diodes D_1 & D_2 are assumed ideal diodes.

For this clipper circuit, when $v_i \leq V_{R1}$, $v_o = V_{R1}$

and, $v_i \geq V_{R2}$, $v_o = V_{R2}$

and, $V_{R1} < v_i < V_{R2}$ $v_o = v_i$

The transfer characteristic of the clipper is shown in **fig. 8.**

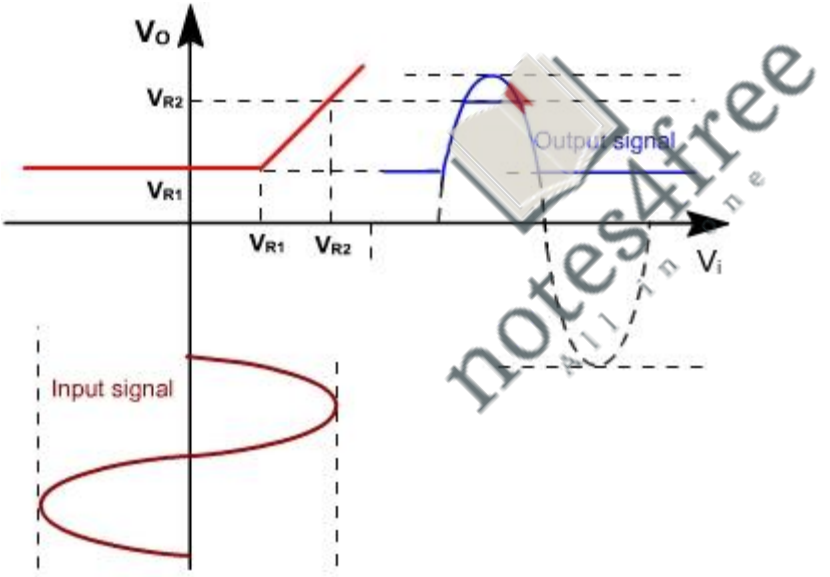


Fig. 8

Example - 1:

Find the output voltage v out of the clipper circuit of **fig. 7(a)** assuming that the diodes are

a. ideal.
b. $V_{on} = 0.7$ V. For both cases, assume R_F is zero.

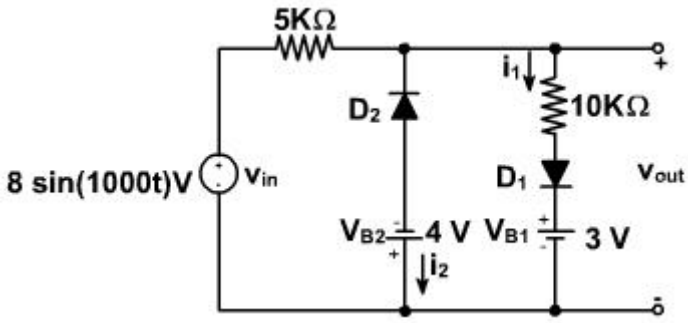


Fig. 7(a)

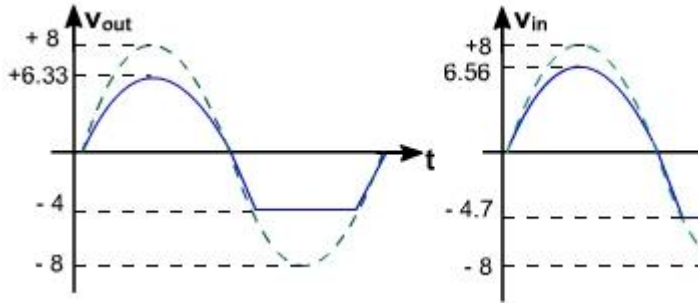


Fig. 7(b)

Solution:

(a). When $v_{in}$is positive and $v_{in} < 3$, then $v_{out} = v_{in}$

and when v_{in} is positive and $v_{in} > 3$, then

$$i_1 = \frac{v_{in} - 3}{1.5 \times 10^4}$$

$$v_{out} = 10^4 i_1 + 3 = \frac{2}{3} v_{in} + 1$$

At v_{in} = 8 V(peak), v_{out} = 6.33 V.

When $v_{in}$is negative and $v_{in} > -4$, then $v_{out} = v_{in}$

When v_{in} is negative and $v_{in} < -4$, then $v_{out} = -4V$

The resulting output wave shape is shown in **fig. 7(b)**.

(b). When V_{ON} = 0.7 V, v_{in} is positive and $v_{in} < 3.7$ V, then $v_{out} = v_{in}$

When $v_{in} > 3.7$ V, then

$$i_1 = \frac{v_{in} - 3.7}{1.5 \times 10^4}$$

$$v_{out} = 10^4 i_1 + 3.7 = \frac{2}{3} v_{in} + 1.23$$

When v_{in} = 8V, v_{out} = 6.56 V.

When v_{in} is negative and $v_{in} > -4.7$ V, then $v_{out} = v_{in}$

When $v_{in} < -4.7$ V, then $v_{out} = -4.7$ V

The resulting output wave form is shown in **fig. 7(b)**.

Clamper Circuits:

Clamping is a process of introducing a dc level into a signal. For example, if the input voltage swings from -10 V and +10 V, a positive dc clamper, which introduces +10 V in the input will produce the output that swings ideally from 0 V to +20 V. The complete waveform is lifted up by +10 V.

Negative Diode clamper:

A negative diode clamper is shown in **fig. 8**, which introduces a negative dc voltage equal to peak value of input in the input signal.

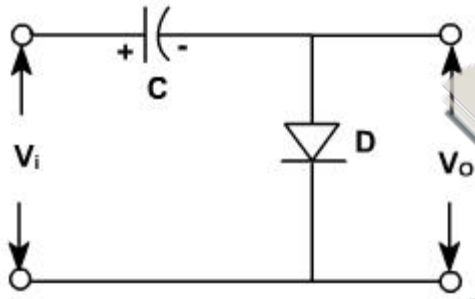


Fig. 8

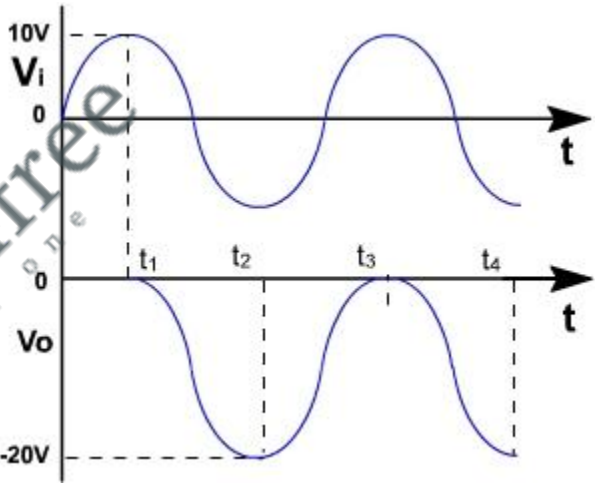


Fig. 9

Let the input signal swings form +10 V to -10 V. During first positive half cycle as V i rises from 0 to 10 V, the diode conducts. Assuming an ideal diode, its voltage, which is also the output must be zero during the time from 0 to t_1. The capacitor charges during this period to 10 V, with the polarity shown.

At that V_i starts to drop which means the anode of D is negative relative to cathode, ($V_D = v_i - v_c$) thus reverse biasing the diode and preventing the capacitor from discharging. **Fig. 9**. Since the capacitor is holding its charge it behaves as a DC voltage source while the diode appears as an open circuit, therefore the equivalent circuit

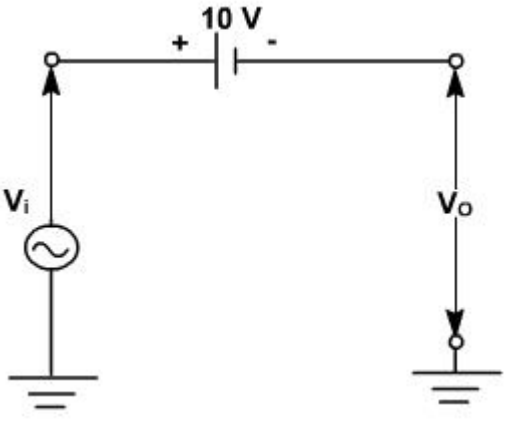


Fig. 10

becomes an input supply in series with -10 V dc voltage as shown in **fig. 10**, and the resultant output voltage is the sum of instantaneous input voltage and dc voltage (-10 V).

Positive Clamper:

The positive clamper circuit is shown in **fig. 1**, which introduces positive dc voltage equal to the peak of input signal. The operation of the circuit is same as of negative clamper.

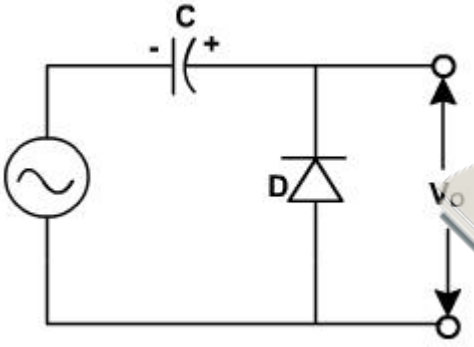


Fig. 1

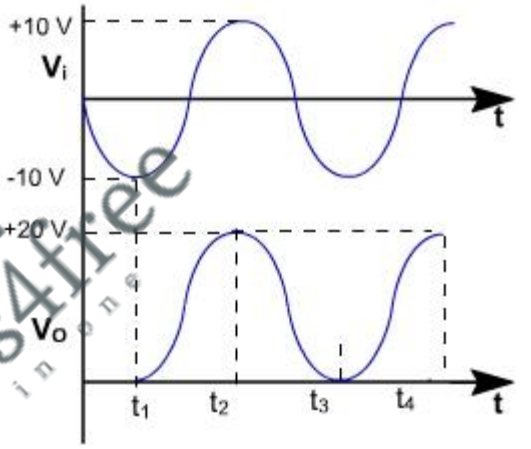


Fig. 2

Let the input signal swings form +10 V to -10 V. During first negative half cycle as V_i rises from 0 to -10 V, the diode conducts. Assuming an ideal diode, its voltage, which is also the output must be zero during the time from 0 to t_1. The capacitor charges during this period to 10 V, with the polarity shown.

After that V_i starts to drop which means the anode of D is negative relative to cathode, ($V_D = v_i - v_C$) thus reverse biasing the diode and preventing the capacitor from discharging. **Fig. 2.** Since the capacitor is holding its charge it behaves as a DC voltage source while the diode appears as an open circuit, therefore the equivalent circuit becomes an input supply in series with +10 V dc voltage and the resultant output voltage is the sum of instantaneous input voltage and dc voltage (+10 V).

To clamp the input signal by a voltage other than peak value, a dc source is required. As shown in **fig. 3**, the dc source is reverse biasing the diode.

The input voltage swings from +10 V to -10 V. In the negative half cycle when the voltage exceed 5V then D conduct. During input voltage variation from ?5 V to -10 V, the capacitor charges to

5 V with the polarity shown in **fig. 3**. After that D becomes reverse biased and open circuited. Then complete ac signal is shifted upward by 5 V. The output waveform is shown in **fig. 4**.

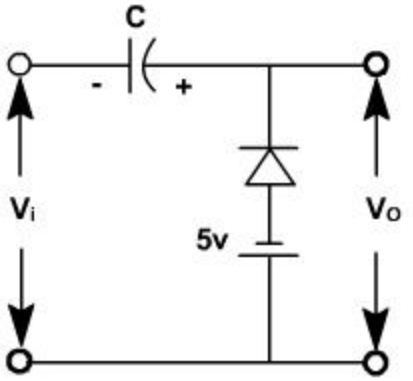


Fig. 3

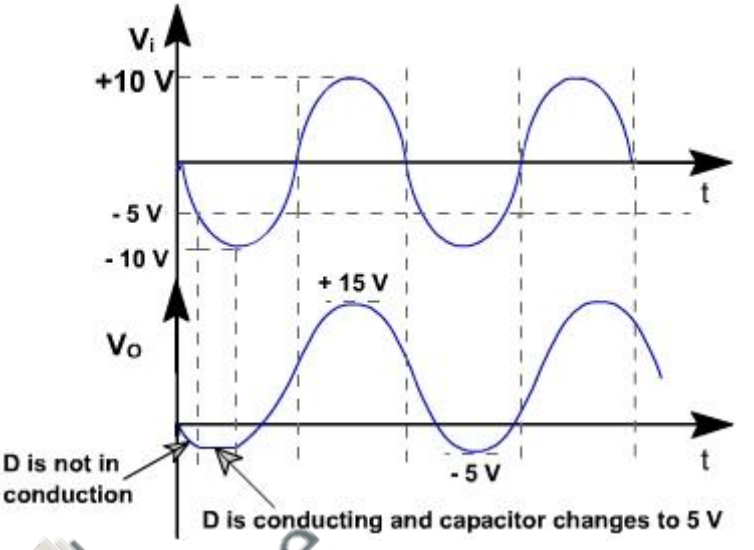


Fig. 4

Voltage Doubler :

A voltage doubler circuit is shown in **fig. 5**. The circuit produces a dc voltage, which is double the peak input voltage.

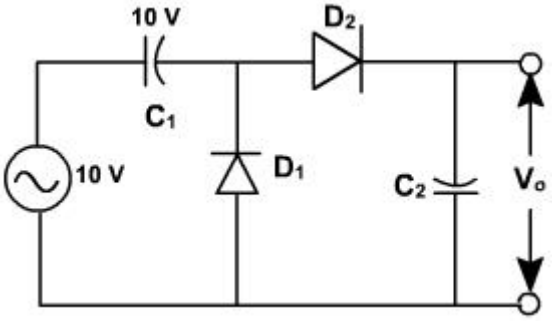


Fig. 5

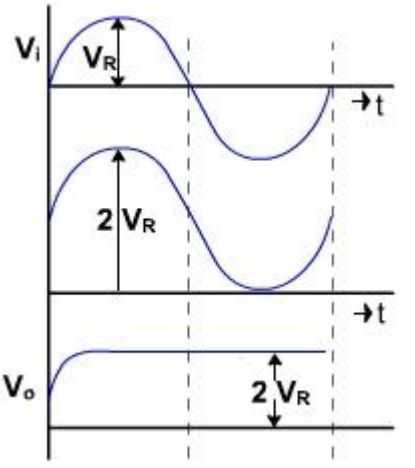


Fig. 6

At the peak of the negative half cycle D_1 is forward based, and D_2 is reverse based. This charges C_1 to the peak voltage V_p with the polarity shown. At the peak of the positive half cycle D_1 is reverse biased and D_2 is forward biased. Because the source and C_1 are in series, C_2 will change toward $2V_p$. e.g. Capacitor voltage increases continuously and finally becomes 20V. The voltage waveform is shown in **fig. 6**.

To understand the circuit operation, let the input voltage varies from -10 V to +10 V. The different stages of circuit from 0 to t_{10} are shown in **fig. 7(a)**.

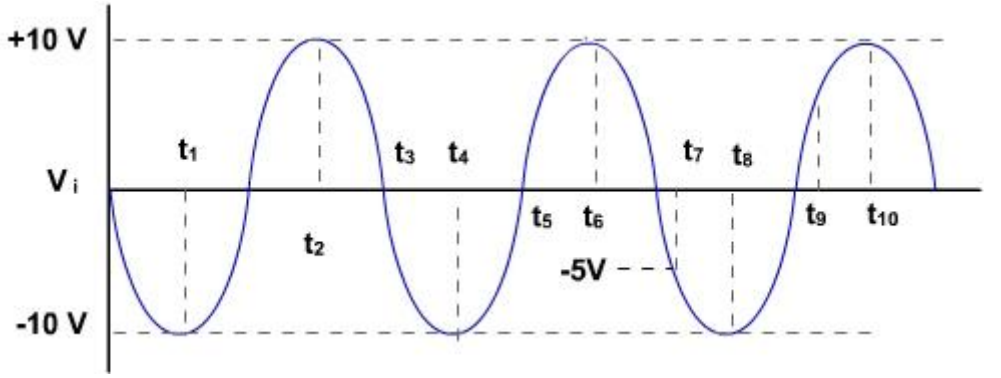


Fig. 7(a)

During 0 to t_1, the input voltage is negative, D_1 is forward biased the capacitor is charged to ?10 V with the polarity as shown in **fig. 7b**.

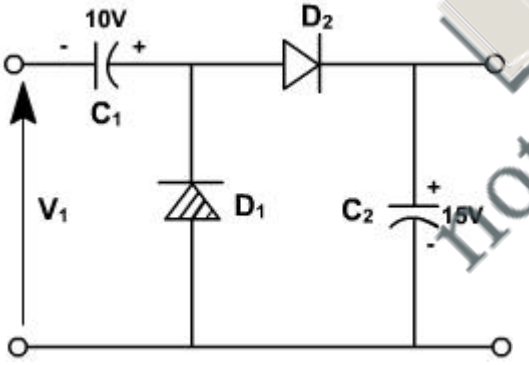


Fig. 7(b)

During t_1 to t_2, D_2 becomes forward biased and conducts and at t_2, when V_i is 10V total voltage change is 20V. If $C_1 = C_2 = C$, both the capacitor voltages charge to +10 V i.e. C_1 voltage becomes 0 and C_2 charges to +10V.

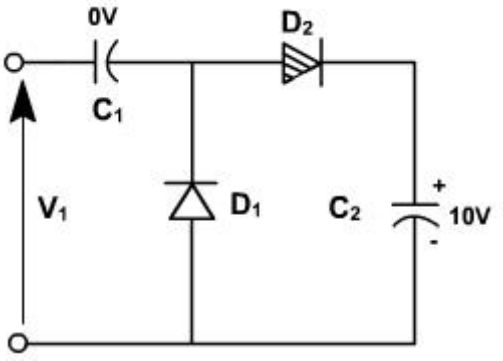


Fig. 7(c)

From t_2 to t_3 there is no conduction as both D_1 and D_2 are reverse biased. During t_3 to t_4 D_1 is forward biased and conducts. C_1 again charges to +10V

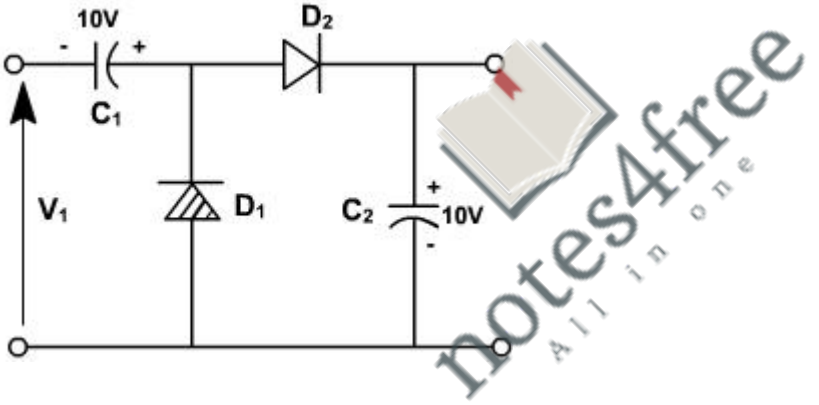


Fig. 7(d)

During t_4 to t_5 both D_1 and D_2 are reverse biased and do not conduct. During t_5 to t_6 D_2 is forward biased and conducts. The capacitor C_2 voltage becomes +15 V and C_1 voltage becomes +5 V.

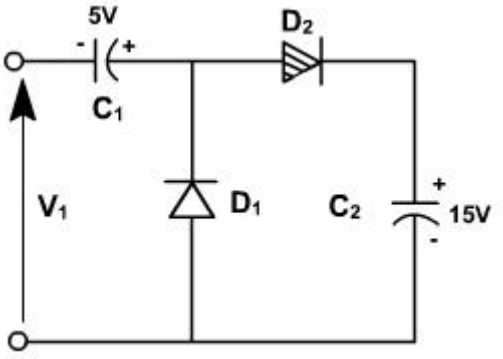


Fig. 7(e)

Again during t_6 to t_7 there is no conduction and during t_7 to t_8, D_1 conducts. The capacitor C_1 recharges to 10 V.

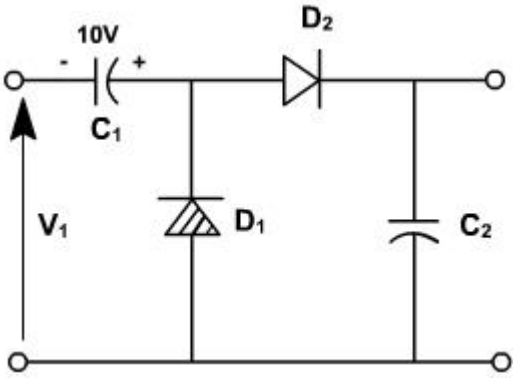


Fig. 7(f)

During t_8 to t_9 both D_1 and D_2 are reverse biased and there is no conduction. During t_9 to t_{10} D_2 conducts and capacitor C_2 voltage becomes + 17.5 V and C_1 voltage becomes 7.5V. This process continues till the capacitor C_1 voltage becomes +20V.

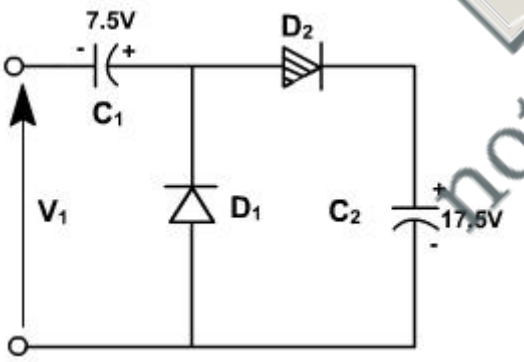


Fig. 7(g)

The power handling capacity of these diodes is better. The power dissipation of a zener diode equals the product of its voltage and current.

$P_Z = V_Z I_Z$

The amount of power which the zener diode can withstand ($V_Z.I_{Z(max)}$) is a limiting factor in power supply design.

Transistor biasing

To Understand :

- Concept of Operating point and stability
- Analyzing Various biasing circuits and their comparison with respect to stability

BJT – A Review

- Invented in 1948 by Bardeen, Brattain and Shockley
- Contains three adjoining, alternately doped semiconductor regions: Emitter (E), Base (B), and Collector (C)
- The middle region, base, is very thin
- Emitter is heavily doped compared to collector. So, emitter and collector are not interchangeable.

Three operating regions

- **Linear** – **region** operation:
  - Base – emitter junction forward biased
  - Base – collector junction reverse biased
- **Cutoff** – **region** operation:
  - Base – emitter junction reverse biased
  - Base – collector junction reverse biased
- **Saturation** – **region** operation:
  - Base – emitter junction forward biased
  - Base – collector junction forward biased

Three operating regions of BJT

- Cut off: $V_{CE} = V_{CC}, I_C \cong 0$

- Active or linear : $V_{CE} \cong V_{CC}/2$, $I_C \cong I_{C\,max}/2$

- Saturation: $V_{CE} \cong 0$, $I_C \cong I_{C\,max}$

Q-Point

- The intersection of the dc bias value of I_B with the dc load line determines the *Q*- point.
- It is desirable to have the *Q*-point centered on the load line. Why?
- When a circuit is designed to have a centered *Q*-point, the amplifier is said to be midpoint biased.
- Midpoint biasing allows optimum ac operation of the amplifier.

Introduction - Biasing

The analysis or design of a transistor amplifier requires knowledge of both the dc and ac response of the system.In fact, the amplifier increases the strength of a weak signal by transferring the energy from the applied DC source to the weak input ac signal

- The analysis or design of any electronic amplifier therefore has two components:
- The dc portion and
- The ac portion

During the design stage, the choice of parameters for the required dc levels will affect the ac response.

What is biasing circuit?

- Once the desired dc current and voltage levels have been identified, a network must be constructed that will establish the desired values of I_B, I_C and V_{CE}, Such a network is known as biasing circuit. A biasing network has to preferably make

use of one power supply to bias both the junctions of the transistor.

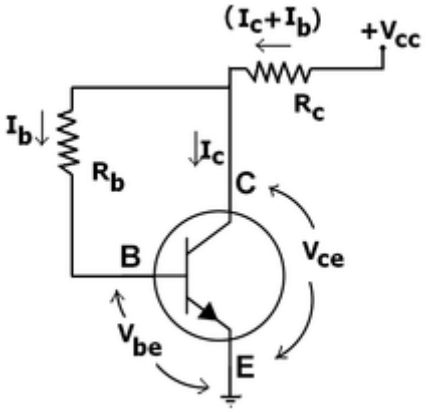
Purpose of the DC biasing circuit

- To turn the device "ON"
- To place it in operation in the region of its characteristic where the device operates most linearly, i.e. to set up the initial dc values of I_B, I_C, and V_{CE}

Important basic relationship

- $V_{BE} = 0.7V$
- $I_E = (\beta + 1)\, I_B \cong I_C$
- $I_C = \beta I_B$

Collector-to-base bias



Collector-to-base bias

This configuration employs negative feedback to prevent thermal runaway and stabilize the operating point. In this form of biasing, the base resistor R_B is connected to the collector instead of connecting it to the DC source V_{CC}. So any thermal runaway will induce a voltage drop across the R_C resistor that will throttle the transistor's base current.

From Kirchhoff's voltage law, the voltage V_{R_b} across the base resistor R_b is

$$V_{R_b} = V_{cc} - \overbrace{(I_c + I_b)R_c}^{\text{Voltage drop across } R_c} - \overbrace{V_{be}}^{\text{Voltage at base}}.$$

By the Ebers–Moll model, $I_c = \beta I_b$, and so

$$V_{R_b} = V_{cc} - (\overbrace{\beta I_b}^{I_c} + I_b)R_c - V_{be} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

From Ohm's law, the base current $I_b = V_{R_b}/R_b$, and so

$$\overbrace{I_b R_b}^{V_{R_b}} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

Hence, the base current I_b is

$$I_b = \frac{V_{cc} - V_{be}}{R_b + (\beta + 1)R_c}$$

If V_{be} is held constant and temperature increases, then the

collector current I_c increases. However, a larger I_c causes the voltage drop across resistor R_c to increase, which in turn reduces the voltage V_{R_b} across the base resistor R_b. A lower base-resistor voltage drop reduces the base current I_b, which results in less collector current I_c. Because an increase in collector current with temperature is opposed, the operating point is kept stable.

Merits:

- Circuit stabilizes the operating point against variations in temperature and β (ie. replacement of transistor)

Demerits:

- In this circuit, to keep I_c independent of β, the following condition must be met:

$$I_c = \beta I_b = \frac{\beta(V_{cc} - V_{be})}{R_b + R_c + \beta R_c} \approx \frac{(V_{cc} - V_{be})}{R_c}$$

which is the case when

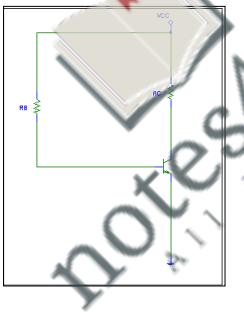
$$\beta R_c \gg R_b.$$

- As β-value is fixed (and generally unknown) for a given transistor, this relation can be satisfied either by keeping R_c fairly large or making R_b very low.
    - If R_c is large, a high V_{cc} is necessary, which increases cost as well as precautions necessary while handling.
    - If R_b is low, the reverse bias of the collector–base region is small, which limits the range of collector voltage swing that leaves the transistor in active mode.
- The resistor R_b causes an AC feedback, reducing the voltage gain of the amplifier. This undesirable effect is a trade-off for greater Q-point stability.

Usage: The feedback also decreases the input impedance of the amplifier as seen from the base, which can be advantageous. Due to the gain reduction from feedback, this biasing form is used only when the trade-off for stability is warranted

Biasing circuits:

- Fixed – bias circuit
- Emitter bias
- Voltage divider bias
- DC bias with voltage feedback
- Miscellaneous bias
- The simplest transistor dc bias configuration.
- For dc analysis, open all the capacitance.



DC Analysis

- Applying KVL to the input loop:

$$V_{CC} = I_B R_B + V_{BE}$$

- From the above equation, deriving for IB, we get,

$$I_B = [V_{CC} - V_{BE}] / R_B$$

- The selection of R_B sets the level of base current for the operating point.
- Applying KVL for the output loop:

$$V_{CC} = I_C R_C + V_{CE}$$

$S(I_{CO}) = \beta + 1$

This indicates poor stability.

Voltage divider configuration

$S(I_{CO}) = (\beta + 1)[1 + R_B / R_E] / [(\beta + 1) + R_B / R_E]$ Here, replace R_B with R_{th}

$S(I_{CO}) = (\beta + 1)[1 + R_{th} / R_E] / [(\beta + 1) + R_{th} / R_E]$

Thus, voltage divider bias configuration is quite stable when the ratio R / R is as small

Physical impact

In a **fixed bias circuit**, I_C increases due to increase in I_{C0}. $[I_C = \beta I_B + (\beta+1) I_{C0}]$

I_B is fixed by V_{CC} and R_B. Thus level of I_C would continue to rise with temperature – a very unstable situation.

In **emitter bias circuit**, **as I_C increases**, I_E increases, V_E increases. Increase in V_E reduces I_B. $I_B = [V_{CC} - V_{BE} - V_E] / R_B$. A drop in I_B **reduces I_C**.Thus, this configuration is such that there is a reaction to an increase in I_C that will tend to oppose the change in bias conditions.

In the **DC bias with voltage feedback**, as I_C increases, voltage across R_C increases, thus reducing I_B and causing I_C to reduce.

The most stable configuration is **the voltage – divider network**. If the condition $\beta R_E >> 10R_2$, the voltage V_B will remain fairly constant for changing levels of I_C. $V_{BE} = V_B - V_E$, as I_C increases, V_E increases, since V_B is constant, V_{BE} drops making I_B to fall, which will try to offset the increases level of I_C.

S(V_{BE})

$S(V_{BE}) = \Delta I_C / \Delta V_{BE}$

For an emitter bias circuit, $S(V_{BE}) = - \beta / [R_B + (\beta + 1)R_E]$

If $R_E = 0$ in the above equation, we get $S(V_{BE})$ for a fixed bias circuit as, $S(V_{BE}) = - \beta / R_B$.

For an emitter bias,

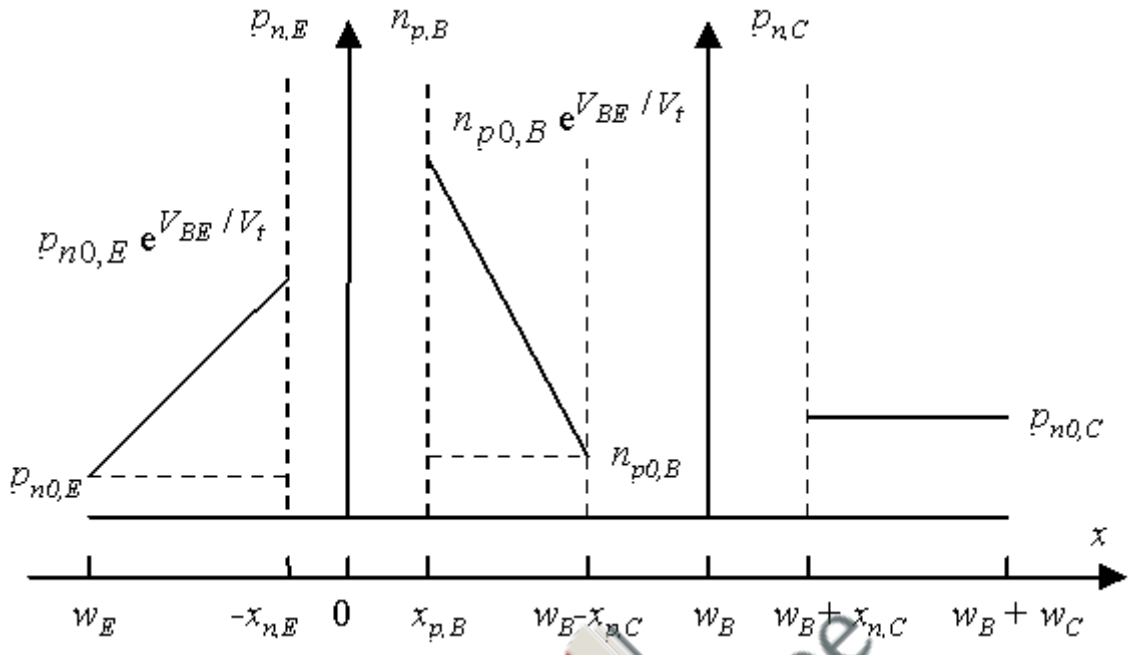
$S(V_{BE}) = - \beta / [R_B + (\beta + 1)R_E]$ can be rewritten as, $S(V_{BE}) = - (\beta/R_E)/ [R_B/R_E + (\beta + 1)]$

If $(\beta + 1) >> R_B/R_E$, then

The larger the R_E, lower the $S(V_{BE})$ and more stable is the system. Total effect of all the three parameters on I_C can be written as,

Forward active mode of operation

The forward active mode is obtained by forward-biasing the base-emitter junction. In addition we eliminate the base-collector junction current by setting $V_{BC} = 0$. The minority-carrier distribution in the quasi-neutral regions of the bipolar transistor, as shown in Figure, is used to analyze this situation in more detail.



Minority-carrier distribution in the quasi-neutral regions of a bipolar transistor (a) Forward active bias mode. (b) Saturation mode.

The values of the minority carrier densities at the edges of the depletion regions are indicated on the Figure. The carrier densities vary linearly between the boundary values as expected when using the assumption that no significant recombination takes place in the quasi-neutral regions. The minority carrier densities on both sides of the base-collector depletion region equal the thermal equilibrium values since V_{BC} was set to zero. While this boundary condition is mathematically equivalent to that of an ideal contact, there is an important difference. The minority carriers arriving at $x = w_B - x_{p,BC}$ do not recombine. Instead, they drift through the base-collector depletion region and end up as majority carriers in the collector region.

$$I_{E,n} = qn_i^2 A_E \left(\frac{D_{n,B}}{N_B w_B'} \right) \left(\exp\left(\frac{V_{BE}}{V_t}\right) - 1 \right)$$

$$I_{E,p} = qn_i^2 A_E \left(\frac{D_{p,E}}{N_E w_E'} \right) \left(\exp\left(\frac{V_{BE}}{V_t}\right) - 1 \right)$$

$$\Delta Q_{n,B} = qA_E \int_{x_{p,E}}^{w_B - x_{p,C}} n_p(x) - n_{p0}\, dx$$

$$\Delta Q_{n,B} = q A_E \frac{n_i^2}{N_B}\left(\exp\left(\frac{V_{BE}}{V_t}\right) - 1\right)\frac{w_B'}{2}$$

And the emitter current due to electrons, $I_{E,n}$, simplifies to:

$$I_{E,n} = \frac{\Delta Q_{n,B}}{t_r}$$

It is convenient to rewrite the emitter current due to electrons, $I_{E,n}$, as a function of the total excess minority charge in the base, $\Delta Q_{n,B}$. This charge is proportional to the triangular area in the quasi-neutral base as shown in Figure and is calculated from

where t_r is the average time the minority carriers spend in the base layer, i.e. the transit time. The emitter current therefore equals the excess minority carrier charge present in the base region, divided by the time this charge spends in the base. This and other similar relations will be used to construct the charge control model of the bipolar junction transistor A combination of equations yields the transit time as a function of the quasi-neutral layer width, w_B', and the electron diffusion constant in the base, $D_{n,B}$.

$$t_r = \frac{w_B'^2}{2D_{n,B}}$$

We now turn our attention to the recombination current in the quasi-neutral base and obtain it from the continuity equation

$$\frac{\partial n_p(x)}{\partial t} = \frac{1}{q}\frac{\partial J_n(x)}{\partial x} - \frac{n_p(x) - n_{p0}}{\tau_n}$$

By applying it to the quasi-neutral base region and assuming steady state conditions:

$$I_{r,B} = qA_E \int_{x_{p,BE}}^{w_B - x_{p,BC}} \frac{n_p(x) - n_{p0}}{\tau_n} dx$$

which in turn can be written as a function of the excess minority carrier charge, $\Delta Q_{n,B}$, using equation

$$I_{r,B} = \frac{\Delta Q_{n,B}}{\tau_n}$$

$$\gamma_E = \frac{1}{1 + \frac{D_{p,E} N_B w_B'}{D_{n,B} N_E w_E'}}$$

It is typically the emitter efficiency, which limits the current gain in transistors made of silicon or germanium. The long minority-carrier lifetime and the long diffusion lengths in those materials justify the exclusion of recombination in the base or the depletion layer. The resulting current gain, under such conditions, is:

$$\beta \cong \frac{D_{n,B} N_E w_E'}{D_{p,E} N_B w_B'}, \quad \text{if} \quad \alpha \cong \gamma_E$$

From this equation, we conclude that the current gain can be larger than one if the emitter doping is much larger than the base doping. A typical current gain for a silicon bipolar transistor is 50 - 150.

$$\alpha_T = 1 - \frac{t_r}{\tau_n} = 1 - \frac{w_B'^2}{2 D_{n,B} \tau_n}$$

This expression is only valid if the base transport factor is very close to one, since it was derived using the "short-diode" carrier distribution. This base transport factor can also be expressed in function of the diffusion length in the base:

$$\alpha_T = 1 - \frac{1}{2}\left(\frac{w_B'}{L_n}\right)^2$$

Uni-junction transistor

The UJT as the name implies, is characterized by a single pn junction. It exhibits negative resistance characteristic that makes it useful in oscillator circuits.

The symbol for UJT is shown in **fig. 1**. The UJT is having three terminals base1 (B1), base2 (B2) and emitter (E). The UJT is made up of an N-type silicon bar which acts as the base as shown in **fig. 2**. It is very lightly doped. A P-type impurity is introduced into the base, producing a single PN junction called emitter. The PN junction exhibits the properties of a conventional diode.

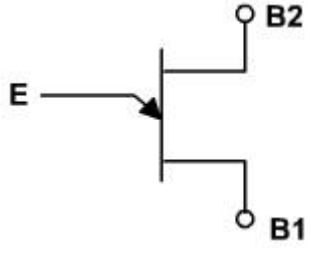


Fig. 1

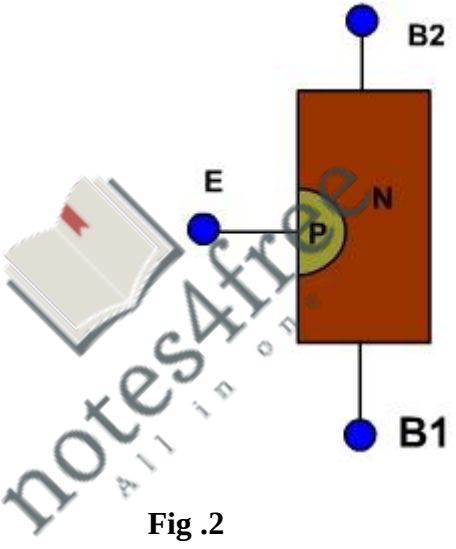


Fig .2

A complementary UJT is formed by a P-type base and N-type emitter. Except for the polarity of voltage and current the characteristic is similar to those of a conventional UJT.

A simplified equivalent circuit for the UJT is shown in **fig. 3**. V_{BB} is a source of biasing voltage connected between B2 and B1. When the emitter is open, the total resistance from B2 to B1 is simply the resistance of the silicon bar, this is known as the inter base resistance R_{BB}. Since the N-channel is lightly doped, therefore R_{BB} is relatively high, typically 5 to 10K ohm. R_{B2} is the resistance between B2 and point ?a', while R_{B1} is the resistance from point ?a' to B1, therefore the interbase resistance R_{BB} is

$R_{BB} = R_{B1} + R_{B2}$

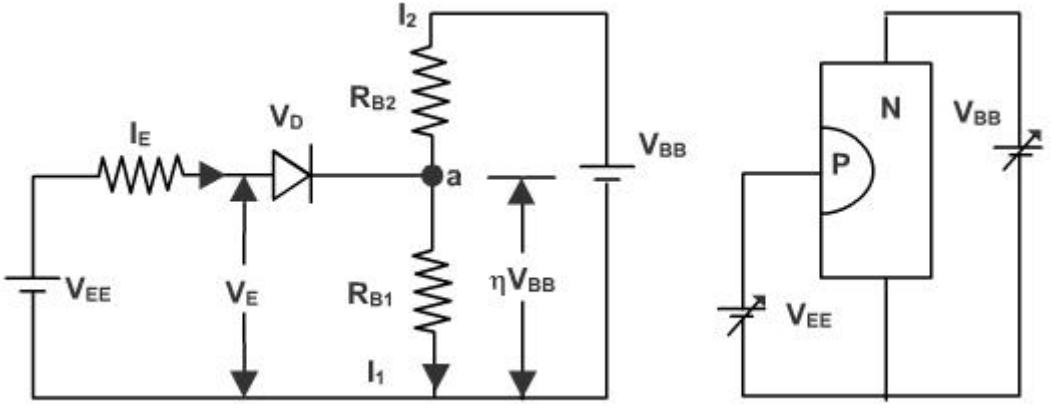


Fig. 3

The diode accounts for the rectifying properties of the PN junction. V_D is the diode's threshold voltage. With the emitter open, $I_E = 0$, and $I_1 = I_2$. The interbase current is given by

$I_1 = I_2 = V_{BB} / R_{BB}$.

Part of V_{BB} is dropped across R_{B2} while the rest of voltage is dropped across R_{B1}. The voltage across R_{B1} is

$V_a = V_{BB} * (R_{B1}) / (R_{B1} + R_{B2})$

The ratio $R_{B1} / (R_{B1} + R_{B2})$ is called intrinsic standoff ratio

$\eta = R_{B1} / (R_{B1} + R_{B2})$ i.e. $V_a = \eta V_{BB}$.

The ratio η is a property of UJT and it is always less than one and usually between 0.4 and 0.85. As long as $I_B = 0$, the circuit of behaves as a voltage divider.

Assume now that v_E is gradually increased from zero using an emitter supply V_{EE} . The diode remains reverse biased till v_E voltage is less than ηV_{BB} and no emitter current flows except leakage current. The emitter diode will be reversed biased.

When $v_E = V_D + \eta V_{BB}$, then appreciable emitter current begins to flow where V_D is the diode's threshold voltage. The value of v_E that causes, the diode to start conducting is called the peak point voltage and the current is called peak point current I_P.

$V_P = V_D + \eta V_{BB}$.

The graph of **fig. 4** shows the relationship between the emitter voltage and current. v_E is plotted on the vertical axis and I_E is plotted on the horizontal axis. The region from $v_E = 0$ to $v_E = V_P$ is called cut off region because no emitter current flows (except for leakage). Once v_E exceeds the peak point voltage, I_E increases, but v_E decreases. up to certain point called valley point (V_V and I_V). This is called negative resistance region. Beyond this, I_E increases with v_E this is the saturation region, which exhibits a positive resistance characteristic.

The physical process responsible for the negative resistance characteristic is called conductivity modulation. When the v_E exceeds V_P voltage, holes from P emitter are injected into N base. Since the P region is heavily doped compared with the N-region, holes are injected to the lower half of the UJT

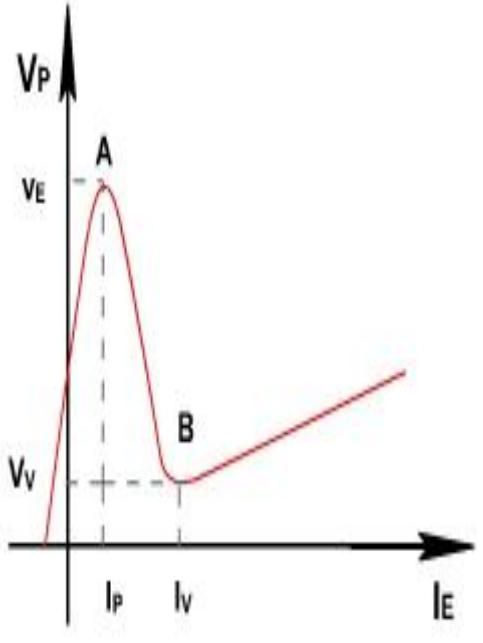


Fig. 4

The lightly doped N region gives these holes a long lifetime. These holes move towards B1 to complete their path by re-entering at the negative terminal of V_{EE}. The large holes create a conducting path between the emitter and the lower base. These increased charge carriers

represent a decrease in resistance R_{B1}, therefore can be considered as variable resistance. It decreases up to 50 ohm.

Since □ is a function of R_{B1} it follows that the reduction of R_{B1} causes a corresponding reduction in intrinsic standoff ratio. Thus as I_E increases, R_{B1} decreases, □ decreases, and V_a decreases. The decrease in V_a causes more emitter current to flow which causes further reduction in R_{B1}, □, and V_a. This process is regenerative and therefore V_a as well as v_E quickly drops while I_E increases. Although R_B decreases in value, but it is always positive resistance. It is only the dynamic resistance between V_V and V_P. At point B, the entire base1 region will saturate with carriers and resistance R_{B1} will not decrease any more. A further increase in I_e will be followed by a voltage rise.

The diode threshold voltage decreases with temperature and R_{BB} resistance increases with temperature because Si has positive temperature coefficient.

UJT Relaxation Oscillator:

The characteristic of UJT was discussed in previous lecture. It is having negative resistance region. The negative dynamic resistance region of UJT can be used to realize an oscillator.

The circuit of UJT relaxation oscillator is shown in **fig. 1**. It includes two resistors R_1 and R_2 for taking two outputs R_2 may be a few hundred ohms and R_1 should be less than 50 ohms. The dc source V_{CC} supplies the necessary bias. The interbase voltage V_{BB} is the difference between V_{CC} and the voltage drops across R_1 and R_2. Usually R_{BB} is much larger than R_1 and R_2 so that V_{BB} approximately equal to V. Note, R_{B1} and R_{B2} are inter-resistance of UJT while R_1 and R_2 is the actual resistor. R_{B1} is in series with R_1 and R_{B2} is in series with R_2 .

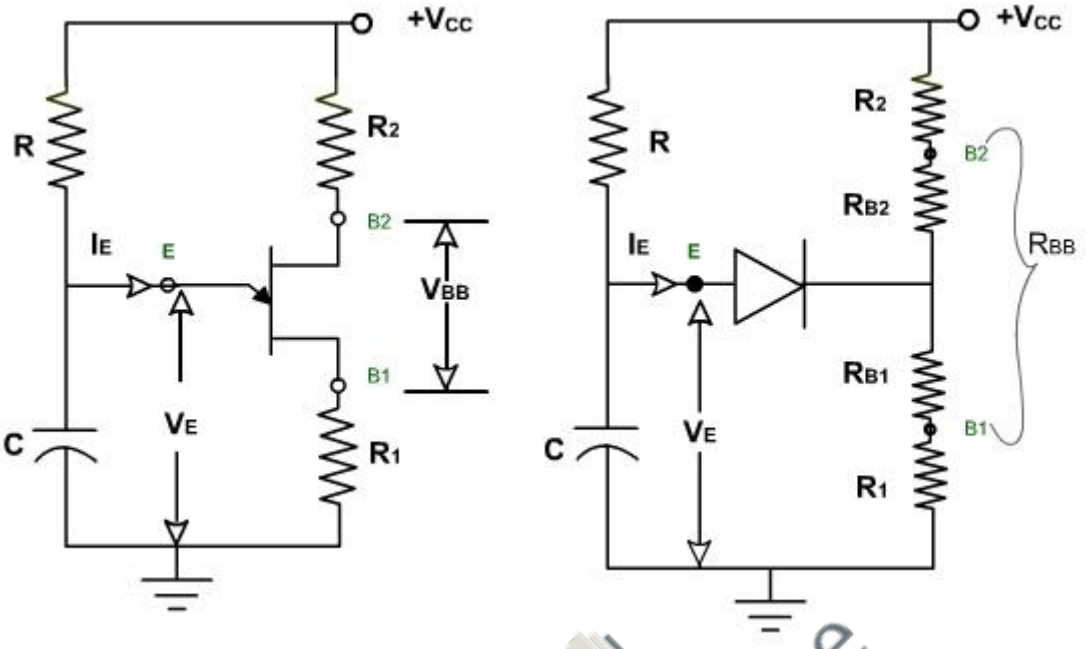


Fig. 1

As soon as power is applied to the circuit capacitor begins to charge toward V. The voltage across C, which is also V_E , rises exponentially with a time constant

$\tau = R C$

As long as $V_E < V_P$, $I_E = 0$. the diode remains reverse biased as long as $V_E < V_P$. When the capacitor charges up to V_P , the diode conducts and R_{B1} decreases and capacitor starts discharging. The reduction in R_{B1} causes capacitor C voltage to drop very quickly to the valley voltage V_V because of the fast time constant due to the low value of R_{B1} and R_1. As soon as V_E drops below $V_a + V_D$ the diode is no longer forward biased and it stops conduction. It now reverts to the previous state and C begins to charge once more toward V_{CC} .

The emitter voltage is shown in **fig. 2**, V_E rises exponentially toward V_{CC} but drops to a very low value after it reaches V_P. The time for the V_E to drop from V_P to V_V is relatively small and usually neglected. The period T can therefore be approximated as follows:

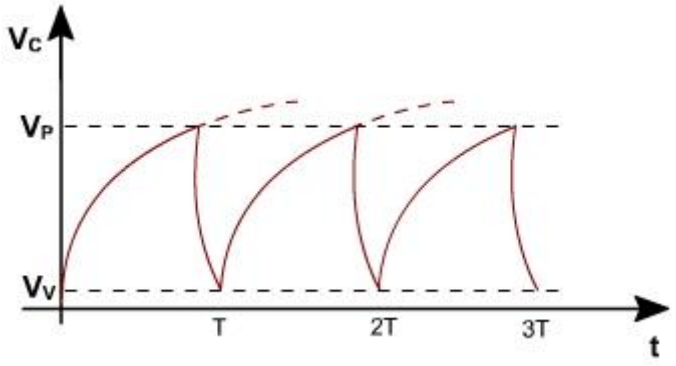


Fig. 2

Let T be the Time required for V_E to rise from 0 to V_P.

As long as $R_{BB} >> (R_1 + R_2)$;

$$V_{BB} \approx V_{CC} \text{ and } V_P = \eta V_{CC}$$

The capacitor charging voltage is given by

$$V_E = V_{CC}(1 - e^{-t/RC})$$

Where V_E is the instantaneous capacitor voltage.

Note that at $t = T$, $V_E = V_P = \eta V_{CC}$

$$\eta V = V_{CC}(1 - e^{-T/RC})$$

or $$\eta = (1 - e^{-T/RC})$$

or $$e^{-T/RC} = 1 - \eta$$

Thus

$$e^{T/RC} = 1/1 - \eta$$

$$T = RC \ln\left(\frac{1}{1-\eta}\right)$$

$$T = RC\ K$$

The frequency of oscillation is, therefore, given by

$$f_C = \frac{1}{T} \frac{1}{RC\ K}$$

The parameter K varies with η

There are two additional outputs possible for the UJT oscillation one of these is the voltage developed at B1 due to capacitor discharge while the other is voltage developed at B2 as shown in **fig. 3**.

When UJT fires (at t = T) V_a drops, causing a corresponding voltage drop at B2. The duration of outputs at B1 and B2 are determined by C discharge time.

If R_1 is very small, C discharges very quickly and very narrow pulse is produced at the output. If $R_1 = 0$, obviously no pulses appear at B1.

If $R_2 = 0$, no pulse can be generated at B2. If R_1 is too large, its positive resistance may swamp the negative resistance and prevent the UJT form switching back after it has fired.

R_2, in addition to providing a source of pulse at B2, is useful for temperature stabilization of the UJT's peak point voltage .

$V_P = V_D + \square\ V_{BB}$.

As the temperature increases, V_p decreases. The temperature coefficient of R_{BB} is positive. R_s is essentially independent of temperature. It is therefore possible to select R_2 so that $\square\ V_{BB}$ increases with temperature by the same amount as V_D decreases. This provides a constant V_P and, in turn, frequency of oscillation.

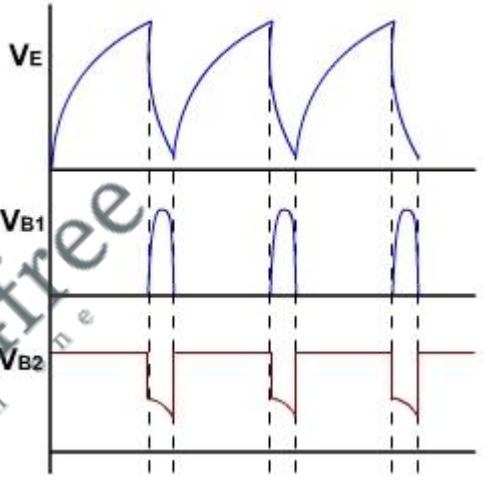


Figure 31.3

Selection of R and C:

In the circuit, R is required to pass only the capacitor charging current. At the instant when V_P is reached; R must supply the peak current. It is therefore, necessary, that the current through R should be slightly greater than the peak point.

$$I_R > I_P$$

$$\frac{V_{CC} - V_P}{R} > I_P$$

$$R < \frac{V_{CC} - V_P}{I_P}$$

Once the UJT fires, V_E drops to the valley voltage V_V . I_E should not be allowed to increases beyond the valley point I_V, otherwise the UJT is taken into saturation region and does not switch back, R therefore must be selected large enough to ensure that

$$I_E < I_V$$

$$\frac{V_{CC} - V_V}{R} < I_V$$

$$R > \frac{V_{CC} - V_V}{I_V}$$

$$\text{Therefore, } \frac{V_{CC} - V_V}{I_P} > R > \frac{V_{CC} - V_V}{I_V}$$

As long as R is chosen between these extremes, reliable operation results.

MODULE -2 Frequency Response of Amplifier

Frequency curve of an RC coupled amplifier:

A practical amplifier circuit is meant to raise the voltage level of the input signal. This signaL may be obtained from anywhere e.g. radio or TV receiver circuit. Such a signal is not of a single frequency. But it consists of a band of frequencies, e.g. from 20 Hz to 20 KHz. If the loudspeakers are to reproduce the sound faithfully, the amplifier used must amplify all the frequency components of signal by same amount. If it does not do so, the output of the loudspeaker will not be the exact replica of the original sound. When this happen then it means distortion has been introduced by the amplifier. Consider an RC coupled amplifier circuit shown in fig. 1.

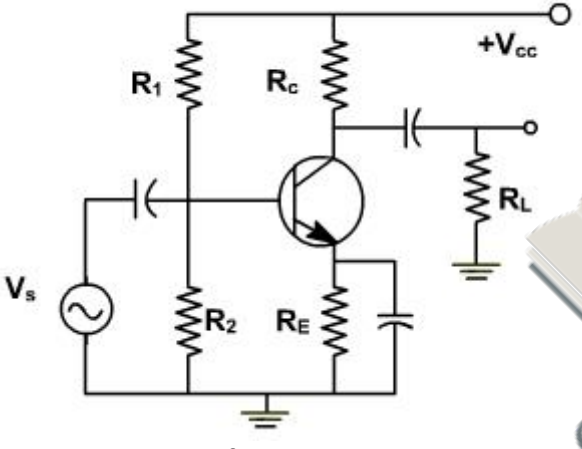


Fig. 1

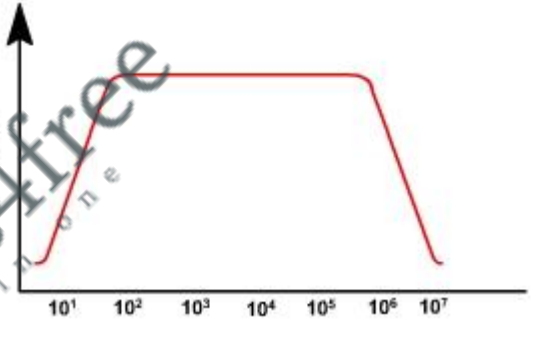


Fig. 2

Fig. 2, shows frequency response curve of a RC coupled amplifier. The curve is usually plotted on a semilog graph paper with frequency range on logarithmic scale so that large frequency range can be accommodated. The gain is constant for a limited band of frequencies. This range is called mid-frequency band and gain is called mid band gain. A_{VM}. On both sides of the mid frequency range, the gain decreases. For very low and very high frequencies the gain is almost zero.

In mid band frequency range, the coupling capacitors and bypass capacitors are as good as short circuits. But when the frequency is low. These capacitors can no longer be replaced by the short circuit approximation.

$$X_C = \frac{1}{2\pi fc}$$

i.e. $X_C \propto \frac{1}{f}$

First consider coupling capacitor. The ac equivalent is shown in **fig. 3**, assuming capacitors are offering some impedance. In mid-frequency band, the capacitors are ac shorted so the input voltage appears directly across r'_e but at low frequency the X_C is significant and some voltage drops across X_C. The input v_{in} at the base decreases. Thus decreasing output voltage. The lower the frequency the more will be X_C and lesser will be the output voltage.

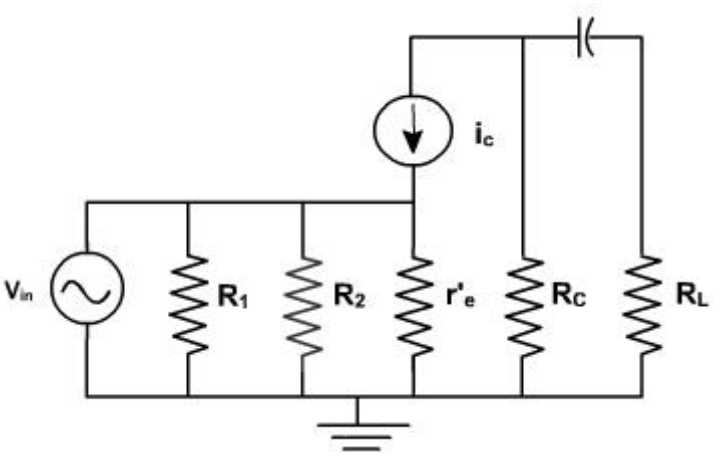
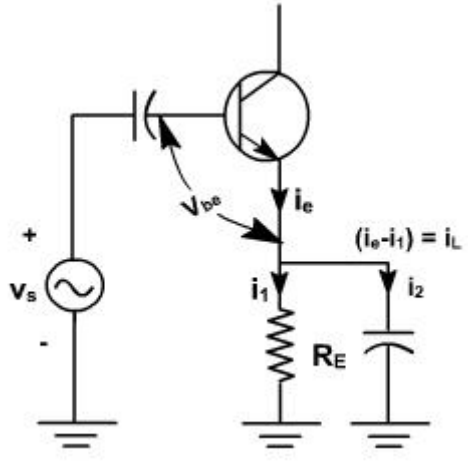


Fig. 3

Similarly at low frequency, output capacitor reactance also increases. The voltage across R_L also reduces because some voltage drop takes place across X_C. Thus output voltage reduces.

The X_C reactance not only reduces the gain but also change the phase between input and output. It would not be exactly 180^o but decided by the reactance. At zero frequency, the capacitors are open circuited therefore output voltage reduces to zero.



The other component due to which gain decreases at low frequencies is the bypass capacitor. The function of this capacitor is to bypass ac and blocks dc The impedence of this capacitor in mid frequency band is very low as compared to R_E so it behaves like ac short but as the frequency decrease the X_{CE} becomes more and no longer behaves like ac short. Now the emitter is not ac grounded. The ac emitter current i.e. divides into two parts i_1 and i_2, as

shown in **fig. 4**. A current i_1 passes through R_E and rest of the current passes through C. Due to ac current i_1 in R_E, an ac voltage is developed $i_1 * R_E$. With the polarity marked at an instant. Thus the effective V_L voltage is given by

$V_{be} = V_s ? R_E$.

Thus the effective voltage input is reduced. The output also reduces. The lower the frequency, the lesser will be the gain. This reduction in gain is due to negative feedback.

As the frequency of the input signal increases, again the gain of the amplifier reduces. Firstly the □ of the transistor decreases at higher frequency. Thus reducing the voltage gain of the amplifier at higher frequencies as shown in **fig. 5**.

The other factor responsible for the reduction in gain at higher frequencies is the presence of various capacitors as shown in **fig. 6**. They are not physically connected but inherently present with the device.

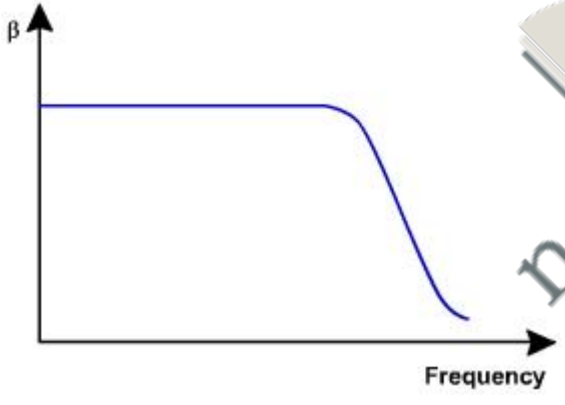


Fig. 5

The capacitor C_{bc} between the base and the collector connects the output with the input. Because of this, negative feedback takes place in the circuit and the gain decreases. This feedback effect is more, when C_{bc} provides a path for higher frequency ac currents

The capacitance C_{be} offers a low input impedance at higher frequency thus reduces the effective input signal and so the gain falls. Similarly, C_{ce} provides a shunting effect at high frequencies in the output side and reduces gain of the amplifier.

Besides these junction capacitances there are wiring capacitance C_{W1} and C_{W2}. These reactance are very small but at high frequencies they become 5 to 20 p.f. For a multistage amplifier,

the effect of the capacitances C_{ce},C_{W1} and C_{W2} can be represented by single shunt capacitance.

$C_S = C_{W1} + C_{W2} + C_{ce}$.

At higher frequency, the capacitor C_S offers low input impedance and thus reduces the output.

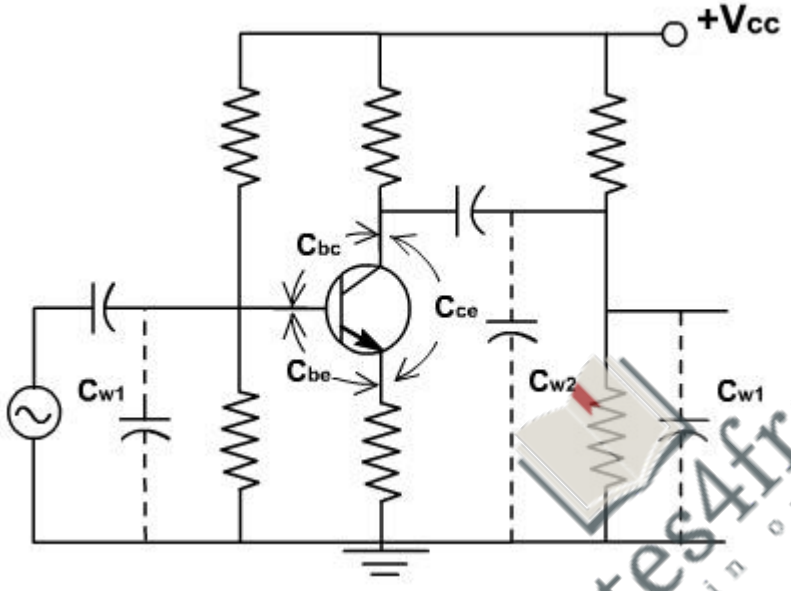


Fig. 6

Bandwidth of an amplifier:

The gain is constant over a frequency range. The frequencies at which the gain reduces to 70.7% of the maximum gain are known as cut off frequencies, upper cut off and lower cut off frequency. **fig. 7**, shows these two frequences. The difference of these two frequencies is called Band width (BW) of an amplifier.

BW = f_2 ? f_1.

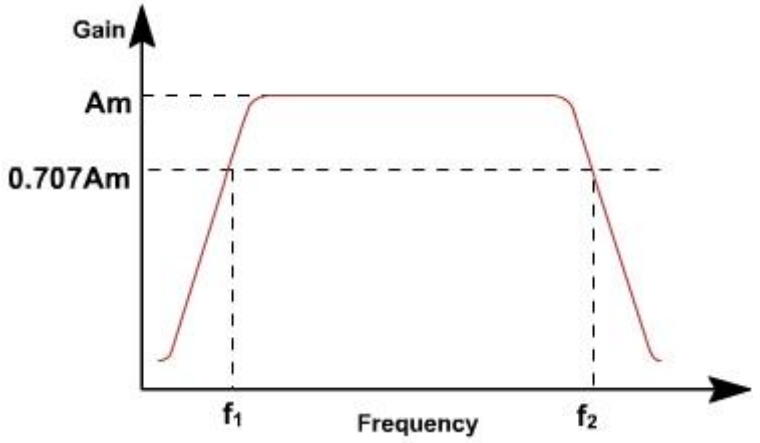


Fig. 7

At f_1 and f_2, the voltage gain becomes 0.707 Am(1 / □ 2). The output voltage reduces to 1 / □ 2 of maximum output voltage. Since the power is proportional to voltage square, the output power at these frequencies becomes half of maximum power. The gain on dB scale is given by

$20 \log_{10}(V_2 / V_1) = 10 \log 10 (V_2 / V_1)^2 = 3$ dB.

$20 \log_{10}(V_2 / V_1) = 20 \log_{10}(0.707) = 10 \log_{10} (1 / □ 2)^2 = 10 \log_{10}(1 / 2) = -3$ dB.

If the difference in gain is more than 3 dB, then it can be detected by human. If it is less than 3 dB it cannot be detected.

Direct Coupling:

For applications, where the signal frequency is below 10 Hz, coupling and bypass capacitors cannot be used. At low frequencies, these capacitors can no longer be treated as ac short circuits, since they offer very high impedance. If these capacitors are used then their values have to be extremely large e.g. to bypass a 100 ohm emitter resistor at 10 Hz, we need a capacitor of approximately 1600□ F. The lower the frequency the worse the problem becomes.

To avoid this, direct coupling is used. This means designing the stages without coupling and bypass capacitors, so that the direct current is coupled as well as alternating current. As a result, there is no lower frequency limit. The amplifier enlarges the signal no matter have low frequency including dc or zero frequency.

One Supply Circuit:

Fig. 8, shows a two stage direct coupled amplifier, no coupling or bypass capacitors are used.

With a quiescent input voltage 1.4 V, emitter voltage = 1.4 - 0.7 = 0.7 V

Emitter current $I_{E1} = \frac{0.7}{680\,\Omega} \approx 1\text{mA}. \therefore \; I_{C1} \approx I_{E1} = 1\text{mA}$

$V_{C1} = 30 - 1*27 = 3\text{V}$

$\therefore V_{E2} = 3 - 0.7 = 2.3\text{V}$

$\therefore I_{E2} = \frac{2.3}{2.4\text{K}} \approx 1\text{mA} \approx I_{C2}$

$\therefore V_{C2} = 30 - 1*24 = 6\text{V}$

The gain of first stage is given by $A_1 = -\frac{2700}{680} \approx -40$

The gain of the second stage is given by

$A_2 = -\frac{24000}{2400} = -10$

$A = A_1 A_2 = 400$

If $V_{in} = 6\,\text{mV}$,

$V_{out} = 5 * 400\text{mV} = 2\text{V}$

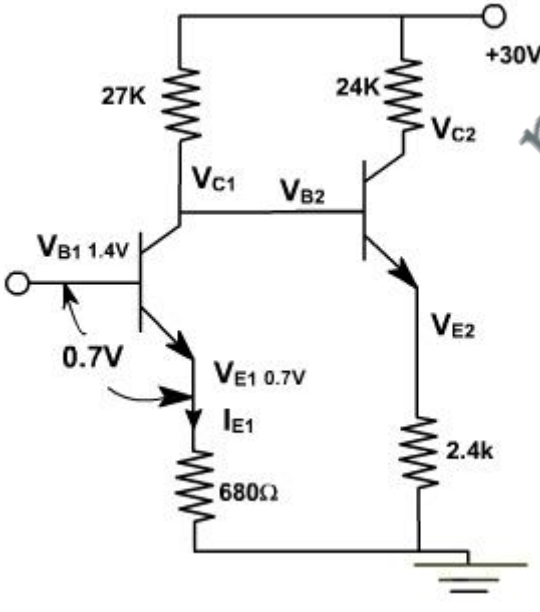


Fig. 8

The output varies from +6V to +8V.

The main disadvantage is variation in transistor characteristic with variation in temperature. This causes I_C and V_C to change. Because of the direct coupling the voltage changes are coupled from one stage to next stage, appearing at the final output as an amplified voltage. The unwanted change is called drift.

Grounded Reference Input

For the above amplifier, we need a quiescent voltage of 1.4V. In most applications, it is necessary to have grounded reference input one where the quiescent input voltage is 0 V, as shown in **fig. 9**.

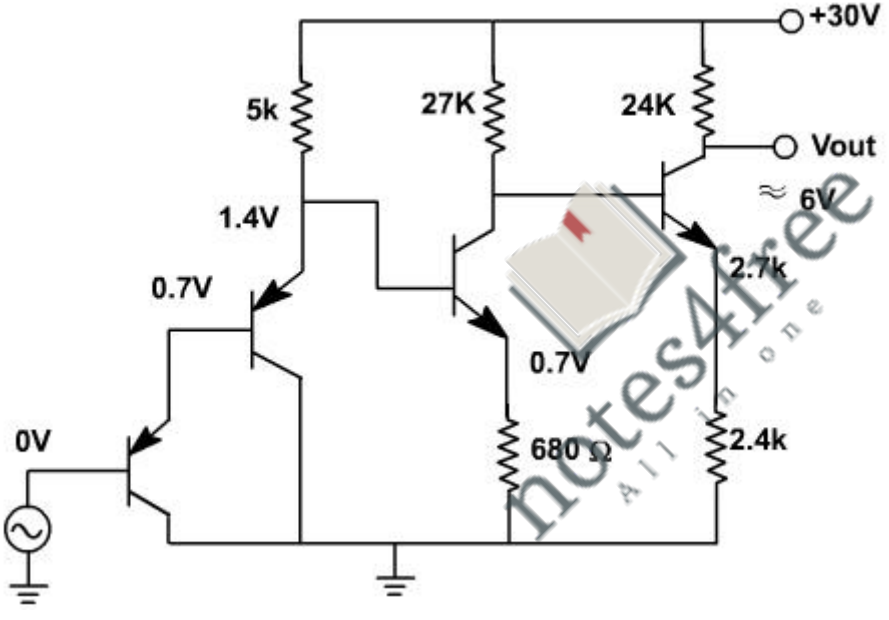


Fig. 9

The quiescent V_{CE} of the first transistor is only 0.7V and the quiescent of the second transistor is only 1.4V. Both the transistors are operating in active region because $V_{CE(sat)}$ is only 0.1 volt. The input is only in mV, which means that these transistors continue to operate in the active region when a small signal is present.

h-Parameters

Small signal low frequency transistor Models:

All the transistor amplifiers are two port networks having two voltages and two currents. The positive directions of voltages and currents are shown in **fig. 1**.

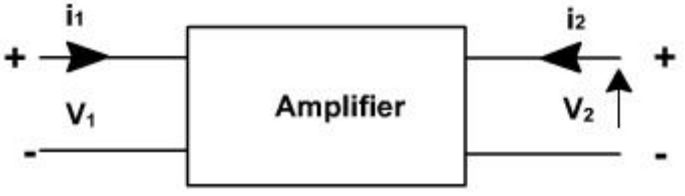


Fig. 1

Out of four quantities two are independent and two are dependent. If the input current i_1 and output voltage v_2 are taken independent then other two quantities i_2 and v_1 can be expressed in terms of i_1 and V_2.

$$v_1 = f_1(i_1, v_2)$$
$$i_2 = f_2(i_1, v_2)$$

The equations can be written as

$$v_1 = h_{11} i_1 + h_{12} v_2$$
$$i_2 = h_{21} i_1 + h_{22} v_2$$

where h_{11}, h_{12}, h_{21} and h_{22} are called h-parameters.

$$h_{11} = \left.\frac{v_1}{i_1}\right|_{v_2 = 0}$$

= h_i = input impedance with output short circuit to ac.

$$h_{12} = \left.\frac{v_1}{v_2}\right|_{i_2 = 0}$$

=h_r = fraction of output voltage at input with input open circuited or reverse voltage gain with input open circuited to ac (dimensions).

$$h_{21} = \left.\frac{i_2}{i_1}\right|_{V_2 = 0}$$

= h_f = negative of current gain with output short circuited to ac.

The current entering the load is negative of I_2. This is also known as forward short circuit current gain.

$$h_{22} = \left.\frac{i_2}{i_1}\right|_{i_2 = 0}$$

= h_o = output admittance with input open circuited to ac.

If these parameters are specified for a particular configuration, then suffixes e,b or c are also included, e.g. h_{fe} ,h_{ib} are h parameters of common emitter and common collector amplifiers

Using two equations the generalized model of the amplifier can be drawn as shown in **fig. 2**.

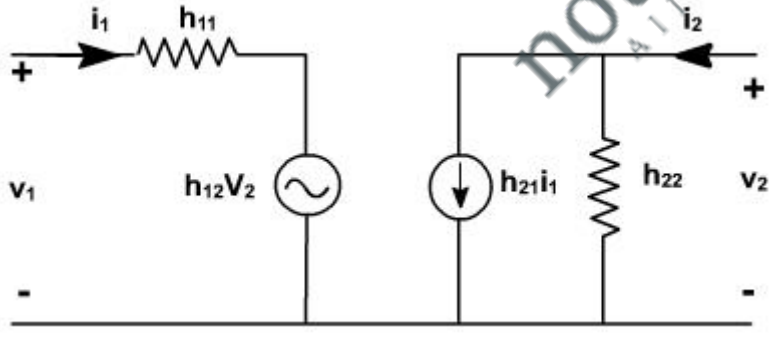


Fig. 2

The hybrid model for a transistor amplifier can be derived as follow:

Let us consider CE configuration as show in **fig. 3**. The variables, i_B, i_C ,v_C, and v_B represent total instantaneous currents and voltages i_B and v_C can be taken as independent variables and v_B, I_C as dependent variables.

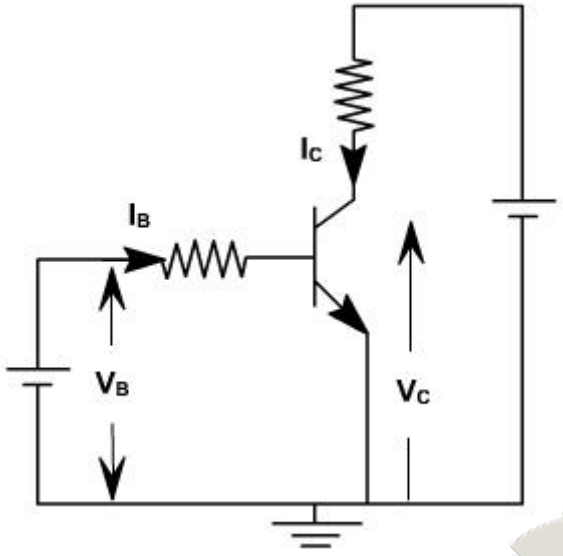


Fig. 3

$v_B = f_1 (i_B ,v_C)$

$I_C = f_2 (i_B , v_C)$.

Using Taylor 's series expression, and neglecting higher order terms we obtain.

$$\Delta v_B = \left.\frac{\partial f_1}{\partial i_B}\right|_{v_C} \Delta i_B + \left.\frac{\partial f_1}{\partial v_C}\right|_{i_B} \Delta v_C$$

$$\Delta i_C = \left.\frac{\partial f_2}{\partial i_B}\right|_{v_C} \Delta i_B + \left.\frac{\partial f_2}{\partial v_C}\right|_{i_B} \Delta v_C$$

The partial derivatives are taken keeping the collector voltage or base current constant. The Δv_B, Δv_C, Δi_B, Δi_C represent the small signal (incremental) base and collector current and voltage and can be represented as v_b ,i_b ,v_C ,i_C.

$$\therefore v_b = h_{ie}\, i_B + h_{re}\, v_C$$
$$i_C = h_{fe}\, i_B + h_{oe}\, v_b$$

where

$$h_{ie} = \left.\frac{\partial f_1}{\partial i_B}\right|_{v_c} = \left.\frac{\partial v_B}{\partial i_B}\right|_{v_c}; \qquad h_{re} = \left.\frac{\partial f_1}{\partial v_C}\right|_{i_B} = \left.\frac{\partial v_B}{\partial v_C}\right|_{i_B}$$

$$h_{fe} = \left.\frac{\partial f_2}{\partial i_B}\right|_{v_c} = \left.\frac{\partial i_C}{\partial i_B}\right|_{v_c}; \qquad h_{oe} = \left.\frac{\partial f_2}{\partial v_C}\right|_{i_B} = \left.\frac{\partial v_B}{\partial v_C}\right|_{i_B}$$

The model for CE configuration is shown in **fig. 4**.

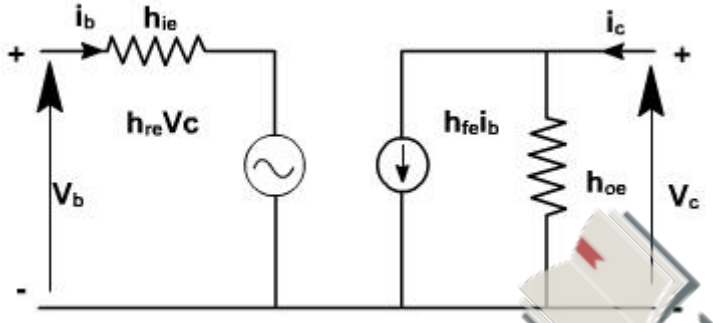


Fig. 4

Determination of h - parameters:

To determine the four h-parameters of transister amplifier, input and output characteristic are used. Input characteristic depicts the relationship between input voltage and input current with output voltage as parameter. The output characteristic depicts the relationship between output voltage and output current with input current as parameter. **Fig. 5**, shows the output characterisitcs of CE amplifier.

$$h_{fe} = \left.\frac{\partial i_C}{\partial i_B}\right|_{V_C} = \frac{i_{C2} - i_{C1}}{i_{b2} - i_{b1}}$$

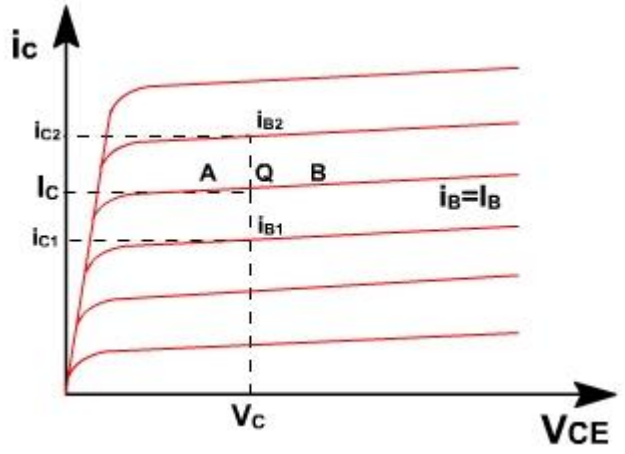


Fig. 5

The current increments are taken around the quiescent point Q which corresponds to $i_B = I_B$ and to the collector voltage $V_{CE} = V_C$

$$h_{oe} = \left.\frac{\partial i_C}{\partial V_C}\right|_{i_B}$$

The value of h_{oe} at the quiescent operating point is given by the slope of the output characteristic at the operating point (i.e. slope of tangent AB).

$$h_{ie} = \frac{\partial V_B}{\partial i_B} \approx \left.\frac{\Delta V_B}{\Delta i_B}\right|_{V_C}$$

h_{ie} is the slope of the appropriate input on **fig. 6**, at the operating point (slope of tangent EF at Q).

$$h_{re} = \frac{\partial V_B}{\partial V_C} = \left.\frac{\Delta V_B}{\Delta V_C}\right|_{I_B} = \frac{V_{B2} - V_{B1}}{V_{C2} - V_{C1}}$$

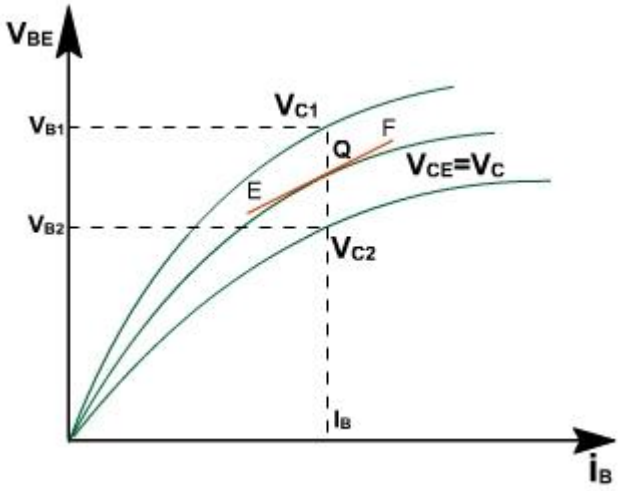


Fig. 6

A vertical line on the input characteristic represents constant base current. The parameter hre can be obtained from the ratio (V_{B2}? V_{B1}) and (V_{C2}? V_{C1}) for at Q.

Typical CE h-parametersof transistor 2N1573 are given below:

h_{ie} = 1000 ohm.
h_{re} = 2.5 * 10 ?4
h_{fe} = 50
h_{oe} = 25 □A / V

Analysis of a transistor amplifier using h-parameters:

To form a transistor amplifier it is only necessary to connect an external load and signal source as indicated in **fig. 1** and to bias the transistor properly.

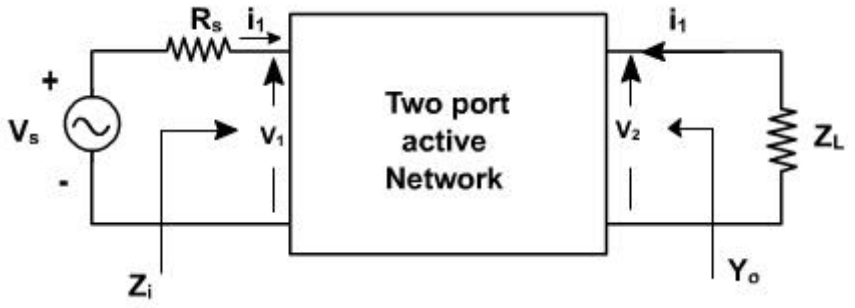


Fig. 1

Consider the two-port network of CE amplifier. R_S is the source resistance and Z_L is the load impedence h-parameters are assumed to be constant over the operating range. The ac equivalent circuit is shown in **fig. 2**. (Phasor notations are used assuming sinusoidal voltage input). The quantities of interest are the current gain, input impedence, voltage gain, and output impedence.

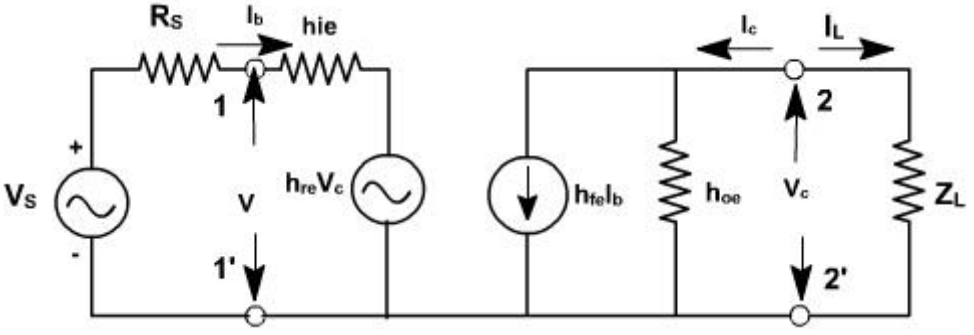


Fig. 2

Current gain:

For the transistor amplifier stage, A_i is defined as the ratio of output to input currents.

$$A_i = \frac{I_L}{I_b} = \frac{-I_C}{I_b} \qquad (I_L + I_c = 0. \quad \therefore I_L = -I_c)$$

$$I_C = h_{fe} I_b + h_{oe} V_c$$

$$V_c = I_L Z_L = -I_c Z_L$$

$$\therefore I_c = h_{fe} I_b + h_{oe} (-I_c Z_L)$$

$$\text{or } \frac{I_c}{I_b} = \frac{h_{fe}}{1 + h_{oe} Z_L}$$

$$\therefore A_i = -\frac{h_{fe}}{1 + h_{oe} Z_L}$$

Input Impedence:

The impedence looking into the amplifier input terminals (1,1') is the input impedence Z_i

$$Z_i = \frac{V_b}{I_b}$$

$$V_b = h_{ie} I_b + h_{re} V_c$$

$$\frac{V_b}{I_b} = h_{ie} + h_{re} \frac{V_c}{I_b}$$

$$= h_{ie} - \frac{h_{re} I_c Z_L}{I_b}$$

$$\therefore Z_i = h_{ie} + h_{re} A_I Z_L$$

$$= h_{ie} - \frac{h_{re} h_{fe} Z_L}{1 + h_{oe} Z_L}$$

$$\therefore Z_i = h_{ie} - \frac{h_{re} h_{fe}}{Y_L + h_{oe}} \qquad (\text{since } Y_L = \frac{1}{Z_L})$$

Voltage gain:

The ratio of output voltage to input voltage gives the gain of the transistors.

$$A_v = \frac{V_C}{V_b} = - \frac{I_C Z_L}{V_b}$$

$$\therefore A_v = \frac{I_B A_i Z_L}{V_b} = \frac{A_i Z_L}{Z_i}$$

Output Admittance:

It is defined as

$$Y_0 = \left.\frac{I_c}{V_c}\right|_{V_s} = 0$$

$$I_c = h_{fe} I_b + h_{oe} V_c$$

$$\frac{I_c}{V_c} = h_{fe}\frac{I_b}{V_c} + h_{oe}$$

when $V_s = 0$, $R_s . I_b + h_{ie} . I_b + h_{re} V_c = 0$.

$$\frac{I_b}{V_c} = -\frac{h_{re}}{R_s + h_{ie}}$$

$$\therefore Y_0 = h_{oe} - \frac{h_{re}\, h_{fe}}{R_s + h_{ie}}$$

Voltage amplification taking into account source impedance (R_S) is given by

$$A_{VS} = \frac{V_c}{V_s} = \frac{V_c}{V_b} * \frac{V_b}{V_S} \qquad \left(V_b = \frac{V_s}{R_s + Z_i} * Z_i\right)$$

$$= A_V \cdot \frac{Z_i}{Z_i + R_s}$$

$$= \frac{A_i\, Z_L}{Z_i + R_s}$$

A_v is the voltage gain for an ideal voltage source ($R_v = 0$).

Consider input source to be a current source I_S in parallel with a resistance R_S as shown in **fig. 3**.

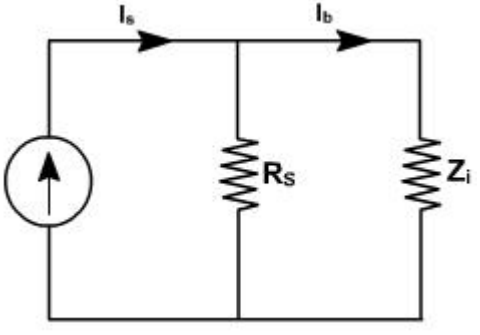


Fig. 3

In this case, overall current gain A_{IS} is defined as

$$A_{I_s} = \frac{I_L}{I_s}$$

$$= -\frac{I_c}{I_s}$$

$$= -\frac{I_c}{I_b} * \frac{I_b}{I_s} \qquad \left(I_b = \frac{I_s * R_s}{R_s + Z_i}\right)$$

$$= A_I * \frac{R_s}{R_s + Z_i}$$

If $R_s \to \infty$, $A_{Is} \to A_I$

To analyze multistage amplifier the h-parameters of the transistor used are obtained from manufacture data sheet. The manufacture data sheet usually provides h-parameter in CE configuration. These parameters may be converted into CC and CB values. For example **fig. 4** h_{rc} in terms of CE parameter can be obtained as follows.

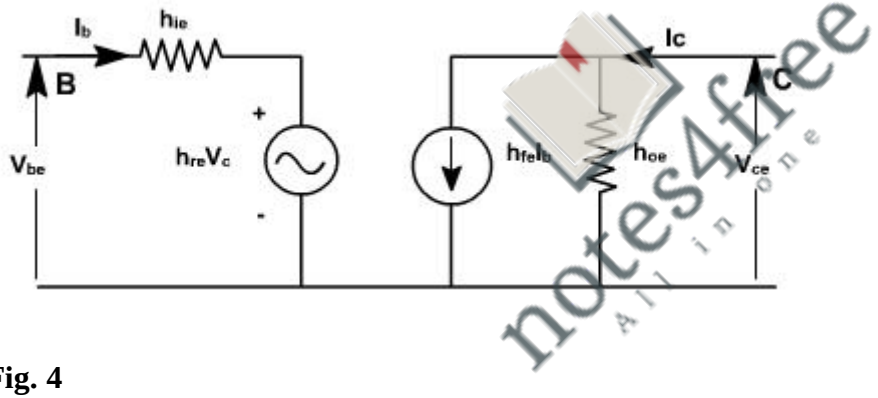


Fig. 4

For CE transistor configuaration

$V_{be} = h_{ie} I_b + h_{re} V_{ce}$

$I_c = h_{fe} I_b + h_{oe} V_{ce}$

The circuit can be redrawn like CC transistor configuration as shown in **fig. 5**.

$V_{bc} = h_{ie} I_b + h_{rc} V_{ec}$

$I_c = h_{fe} I_b + h_{oe} V_{ec}$

$$h_{rc} = \left.\frac{V_{be}}{V_{ec}}\right|_{I_b=0}$$

$$= \left.\frac{V_{be}+V_{ec}}{V_{ec}}\right|_{I_b=0}$$

$$= \left.\left(\frac{V_{be}}{V_{ec}}+1\right)\right|_{I_b=0}$$

Since $I_b = 0$, $V_{be} = h_{re} V_c = -h_{re} V_{ec}$

$$\therefore h_{rc} = 1+\left(\frac{h_{re} V_{ec}}{V_{ec}}\right)$$

$$= 1 - h_{re}$$

Similarly

$$h_{fc} = \left.\frac{I_e}{I_b}\right|_{V_{ec}=0} = \left.\frac{-(I_b+I_C)}{I_b}\right|_{V_{ec}=0}$$

$$= -(1+h_{fe})$$

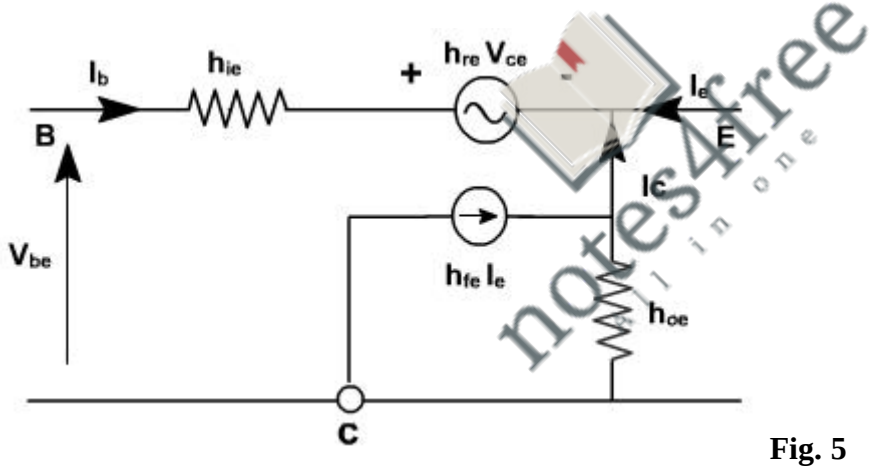


Fig. 5

Example - 1

For the circuits shown in **fig. 1**. (CE?CC configuration) various h-parameters are given

h_{ie} = 2K, h_{fe} = 50, h_{re} = 6 * 10^{-4}, h_{oc}= 25 □ A/ V.

h_{ic} = 2K, h_{fe} = -51, h_{re} = 1, h_{oc} = 25 □ A/ V.

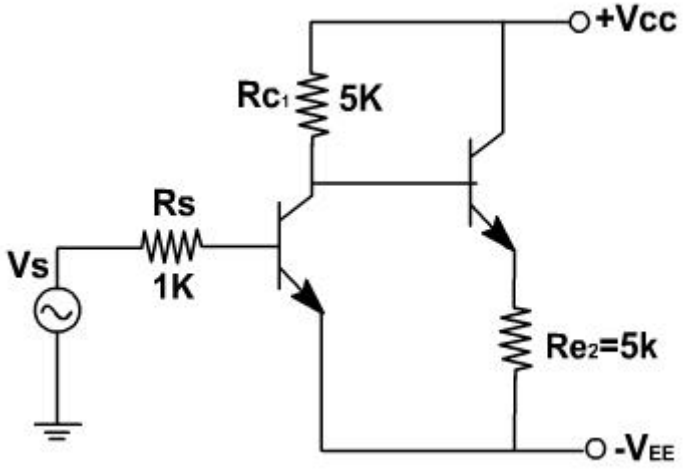


Fig. 1

The small signal model of the transistor amplifier is shown in **fig. 2.**

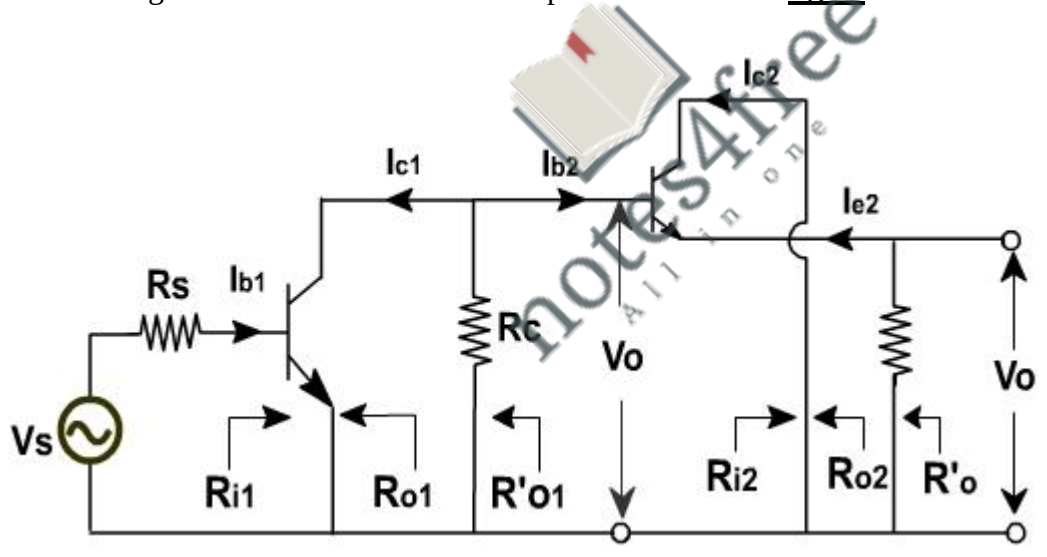


Fig. 2

In the circuit, the collector resistance of first stage is shunted by the input impedence of last stage. Therefore the analysis is started with last stage. It is convenient; to first compute current gain, input impedence and voltage gain. Then output impedence is calculated starting from first stage and moving towards end.

$$A_{i2} = \frac{-h_{fe}}{1+h_{oc}Z_L} = \frac{51}{1+25*10^{-6}*5*10^3}$$
$$= 45.3$$

$$R_{i2} = h_{ic} + h_{rc}A_{i2}Z_L$$
$$= 2*10^3 + 1*45.3*5*10^3$$
$$= 228.5K \text{ (high input impedence)}$$

$$A_{V2} = \frac{V_0}{V_2} = \frac{A_i Z_L}{Z_{i2}}$$
$$= \frac{45.3*5}{228.5} = 0.99 \approx 1$$

$$R_{L1} = R_{C1} \| R_{i2}$$
$$= \frac{5*228.5}{5+228.5} = 4.9K$$

$$A_{i1} = -\frac{h_{fe}}{1+h_{oe}R_L} = \frac{-50}{1+25*10^{-6}*4.9*10^3}$$
$$= 44.5$$

$$R_{i1} = h_{ie} + h_{re}A_{i1}R_{L1}$$
$$= 2 - 6*10^{-4}*44.5*4.9$$
$$= 1.87K$$

Voltage gain of first stage is

$$A_{V1} = \frac{A_{i1}R_{L1}}{R_{i1}} = \frac{-44.5*4.9}{1.87}$$
$$= -116.6$$

$$Y_{o1} = h_{oe} - \frac{h_{fe}\,h_{re}}{h_{ie}+R_s}$$
$$= 25*10^{-6} - \frac{50*6*10^{-4}}{2*10^3+1*10^3}$$
$$= 15*10^{-6} \text{ mho}$$

$$R_{o1} = \frac{1}{Y_{o1}} = 66.7K$$

$$R'_{o1} = R_{o1} \| R_{c1}$$
$$= 66.7 \| 5$$
$$= 4.65K$$

The effective source resistance R'_{S2} for the second stage is $R_{01} \| R_{C1}$. Thus $R_{S2} = R'_{01} = 4.65K$

$$Y_{02} = h_{oe} - \frac{h_{fe}\, h_{rc}}{h_{ic} + R_{S2}}$$

$$= 25*10^{-6} - \frac{(-51)(1)}{2*10^{3} + 4.65*10^{3}}$$

$$= 7.70*10^{-3}\ \text{A/V}$$

$$R_{02} = \frac{1}{Y_{02}} = 130\,\Omega$$

$$R'_{02} = R_{02} \,||\, R_{c2}$$

$$= 0.13 \,||\, 5K$$

$$= 127\,\Omega$$

Overall current gain of the amplifier is A_i and is given by

$$A_i = -\frac{I_{e2}}{I_{b1}}$$

$$= -\frac{I_{e2}}{I_{b2}} * \frac{I_{b2}}{I_{c1}} * \frac{I_{c1}}{I_{b1}}$$

$$= -A_{i2} \cdot \frac{I_{b2}}{I_{c1}} * A_{i1}$$

The equivalent circuit of the amplifier is shown in **fig. 3**. From the circuit it is clear that the current i_{c1} is divided into two parts.

Therefore,

$$\frac{I_{b2}}{I_{c1}} = \frac{-R_{c1}}{R_{c1} + R_{i2}}$$

and

$$\therefore A_I = A_{i2} \cdot A_{i1} \cdot \frac{R_{c1}}{R_{c1} + R_{i2}}$$

$$= 45.3 * (-44.5) * \frac{5}{228.5 + 5} = -43.2$$

$$A_V = \frac{V_0}{V_I} = \frac{V_0}{V_2} \cdot \frac{V_2}{V_1}$$

$$= A_{V2} \cdot A_{V1}$$

$$= 0.99 * (-11.6)$$

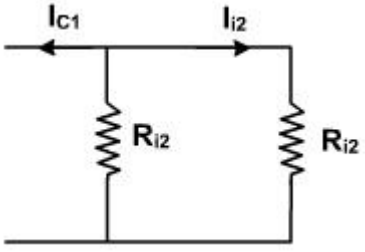
$$= 115$$

Overall voltage gain of the amplifier is given by

$$A_{VS} = \frac{V_0}{V_S} = A_V \cdot \frac{R_{i1}}{R_{i1} + R_S}$$

$$= -115 * \frac{1.87}{1.87 + 1}$$

$$= -75.3$$



Simplified common emitter hybrid model:

In most practical cases it is appropriate to obtain approximate values of A_V , A_i etc rather than calculating exact values. How the circuit can be modified without greatly reducing the accuracy. **Fig. 4** shows the CE amplifier equivalent circuit in terms of h-parameters Since 1 / h_{oe} in parallel with R_L is approximately equal to R_L if 1 / h_{oe} >> R_L then h_{oe} may be neglected. Under these conditions.

$I_c = h_{fe} I_B$.

$h_{re} v_c = h_{re} I_c R_L = h_{re} h_{fe} I_b R_L$.

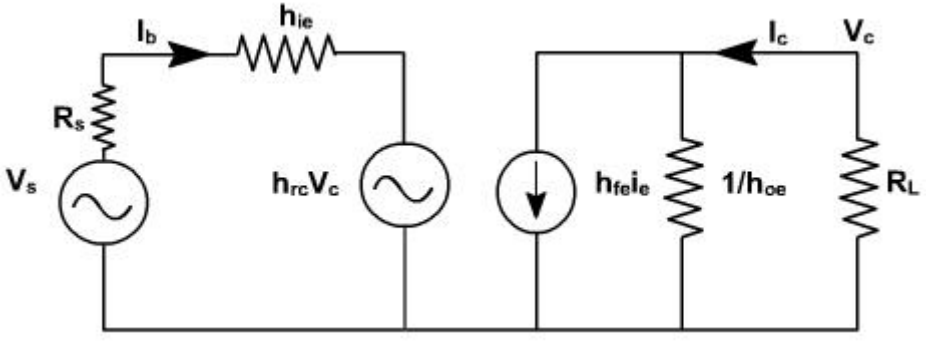


Fig. 4

Since $h_{fe}.h_{re} \square 0.01$, this voltage may be neglected in comparison with $h_{ic} I_b$ drop across h_{ie} provided R_L is not very large. If load resistance R_L is small than hoe and h_{re} can be neglected.

$$A_I = -\frac{h_{fe}}{1+h_{oe} R_L} \approx -h_{fe}$$

$$R_i = h_{ie}$$

$$A_V = \frac{A_I R_L}{R_i} = -\frac{h_{fe} R_L}{h_{ie}}$$

Output impedence seems to be infinite. When $V_s = 0$, and an external voltage is applied at the output we fined $I_b = 0$, $I_C = 0$. True value depends upon R_S and lies between 40 K and 80K.

On the same lines, the calculations for CC and CB can be done.

CE amplifier with an emitter resistor:

The voltage gain of a CE stage depends upon h_{fe}. This transistor parameter depends upon temperature, aging and the operating point. Moreover, h_{fe} may vary widely from device to device, even for same type of transistor. To stabilize voltage gain A_V of each stage, it should be independent of h_{fe}. A simple and effective way is to connect an emitter resistor R_e as shown in **fig. 5**. The resistor provides negative feedback and provide stabilization.

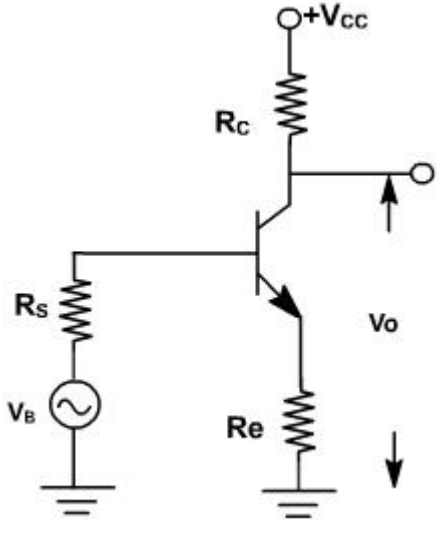


Fig. 5

An approximate analysis of the circuit can be made using the simplified model.

$$\text{Current gain } A_i = \frac{I_L}{I_b} = -\frac{I_C}{I_b} = -\frac{h_{fe}\, I_b}{I_b}$$
$$= -h_{fe}$$

It is unaffected by the addition of R_C.

Input resistance is given by

$$R_i = \frac{V_i}{I_b}$$
$$= \frac{h_{ie}\, I_b + (1+h_{fe})\, I_b\, R_e}{I_b}$$
$$= h_{ie} = (1+h_{fe})\, R_e$$

The input resistance increases by $(1+h_{fe})\, R_e$

$$A_v = \frac{A_i R_L}{R_i} = \frac{-h_{fe}\, R_L}{h_{ie} + (1+h_{fe}) R_e}$$

Clearly, the addition of R_e reduces the voltage gain.

If $(1+h_{fe})R_e >> h_{ie}$ and $h_{fe} >> 1$

then

$$A_v = \frac{-h_{fe}\, R_L}{(1+h_{fe})R_e} \approx -\frac{R_L}{R_e}$$

Subject to above approximation A_V is completely stable. The output resistance is infinite for the approximate model.

Module-3

General Amplifiers

Darlington Amplifier:

It consists of two emitter followers in cascaded mode as shown in **fig. 1**. The overall gain is close to unity. The main advantage of Darlington amplifier is very large increase in input impedence and an equal decrease in output impedance **.**

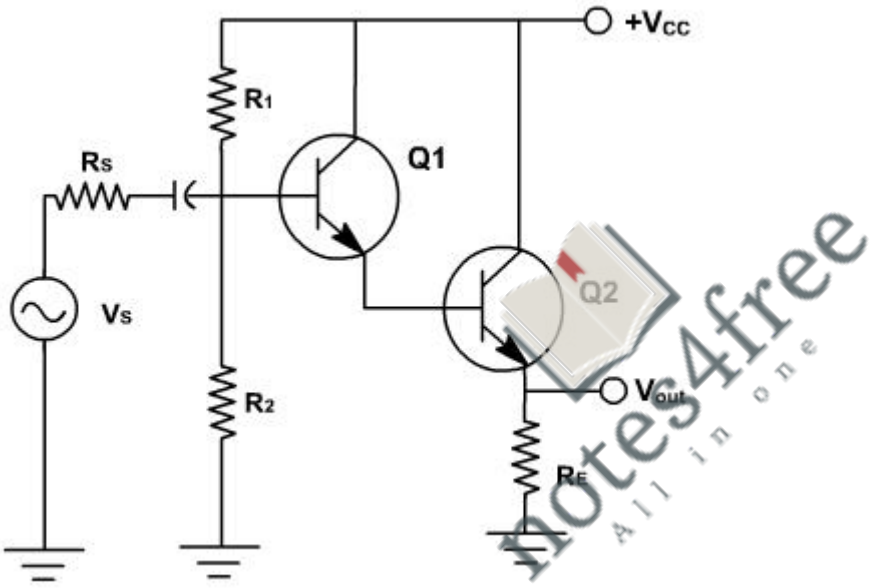


Fig. 1

DC Analysis:

The first transistor has one V_{BE} drop and second transistor has second V_{BE} drop. The voltage divider produces V_{TH} to the input base. The dc emitter current of the second stage is

$I_{E2} = (V_{TH} ? 2\ v_{BE}) / (R_E)$

The dc emitter current of the first stage that is the base current of second stage is given by

$I_{E1} \square I_{E2}./\square_2$

If $r'_{e(2)}$ is neglected then input impedance of second stage is

$Z_{in\,(2)} = \beta_2 R_E$

This is the impedance seen by the first transistor. If $r'_{e(1)}$ is also neglected then the input impedance of 1 becomes.

$Z_{in\,(1)} = \beta_1 \beta_2 R_E$

which is extremely high because of the products of two betas, so the approximate input impedance of Darlington amplifier is

$Z_{in} = R_1 \parallel R_2$

Output impedance:

The Thevenin impedance at the input is given by

$R_{TH} = R_S \parallel R_1 \parallel R_2$

Similar to single stage common collector amplifier, the output impedance of the two stages $z_{out(1)}$ and $z_{out(2)}$ are given by.

$$z_{out1} = r'_{e1} + \frac{R_{TH}}{\beta_1}$$

$$z_{out2} = r'_{e2} + \frac{z_{out1}}{\beta_2}$$

$$= r'_{e2} + \frac{r'_{e1} + \frac{R_{TH}}{\beta_1}}{\beta_2}$$

Therefore, t he output impedance of the amplifier is very small.

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$$z_{out2} = r'_{e2} + \frac{z_{out1}}{\beta_2}$$

$$= r'_{e2} + \frac{r'_{e1} + \frac{R_{TH}}{\beta_1}}{\beta_2}$$

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$$z_{out2} = r'_{e2} + \frac{z_{out1}}{\beta_2}$$

$$= r'_{e2} + \frac{r'_{e1} + \frac{R_{TH}}{\beta_1}}{\beta_2}$$

Therefore, t he output impedance of the amplifier is very small. **Output impedance:**

The Thevenin impedance at the input is given by

$R_{TH} = R_S \parallel R_1 \parallel R_2$

Similar to single stage common collector amplifier, the output impedance of the two stages $z_{out(1)}$ and $z_{out(2)}$ are given by.

$$z_{out1} = r'_{e1} + \frac{R_{TH}}{\beta_1}$$

$$z_{out2} = r'_{e2} + \frac{z_{out1}}{\beta_2}$$

$$= r'_{e2} + \frac{r'_{e1} + \frac{R_{TH}}{\beta_1}}{\beta_2}$$

Therefore, t he output impedance of the amplifier is very small.

Efficiency is given by

$$\eta\% = \frac{P_{OUT}}{P_{DC}} \times 100$$

Value is around 40%

Example-1

Design a single stage npn emitter follower amplifier as shown in **fig. 2** with $\beta = 60$, $V_{BE} = 0.7V$, $R_{source} = 1\ K\Omega$, and $V_{CC} = 12V$. Determine the circuit element values for the stage to achieve $A_i = 10$ with a $100\ \Omega$ load.

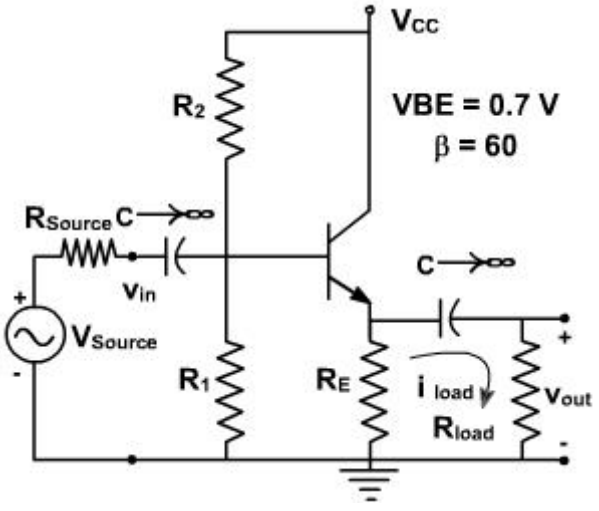


Fig. 2

Solution:

We must select R_1, R_2 and R_E, but we only have two equations. These two equations are specified by the current gain and the placement of the Q-point.

As discussed earlier, the best choice for a CE amplifier is to make $R_C = R_{load}$. We could derive a similar result for R_E and R_{load} in the CC amplifier. We shall therefore begin by constraining R_E to be equal to R_{load}. This yields a third equation,

$R_E = R_{load} = 100$ W

Now finding the load line slopes,

$R_{ac} = R_E \parallel R_{load} = 50$ W

$R_{dc} = R_E = 100$ V

Since the amplitude of the input is not specified, we choose the quiescent current to place the Q-point in the center of the ac load line for maximum swing.

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}} = 80 \text{ mA}$$

$$V_{CEQ} = I_{CQ} R_{ac} = 4 \text{ V}$$

We now find the value of r'_e

$$r_e' = \frac{25\ (mV)}{|I_{CQ}|} = \frac{25\ (mV)}{80\ (mA)} = 0.313\Omega$$

Since r_e is insignificant compared to $R_E \parallel R_{load}$, it can be ignored. This is usually the case for emitter follower circuits.

Using the equation for current gain we find

$$A_i = \frac{\beta R_E R_B}{(R_E + R_{load})[R_B + (R_E \parallel R_{load})\beta]}$$

Everything in this equation is known except R_B. We solve for R_B with the result

$R_B = 1500$ W

V_{BB} is found from the base loop.

$$V_{BB} = V_{BE} + I_{CQ}\left(\frac{R_B}{\beta} + R_E\right) = 10.7\ V$$

Continuing with the design as discussed earlier, we find

$R_1 = 13.8$ K Ω

$R_2 = 1.68$ K Ω

The voltage gain of the CC amplifier is approximately unity.

The input resistance is given by

$R_{in} = R_B \parallel [\ \beta\ (\ R_E \parallel R_{load}\ )\ ] = 1$ kΩ

The output resistance is given by

$$R_O = \left(\frac{R_s + R_{source} \parallel R_B}{\beta}\right) \parallel R_E = 9.36\Omega$$

The maximum peak to peak symmetrical output swing is given by

$V_{out}(p\text{-}p) \approx 1.8 \, |I_{CQ}| \, (R_E \parallel R_{load}) = 7.2$ V

The power dissipated in the load, P_{load}, and the maximum power required of the transistor, $P_{transistor}$, are

$$P_{load} = \frac{(0.9 I_{CQ}/2)^2 R_{load}}{2} = 64.8 \text{ mW}$$

$$P_{transistor} = I_{CQ} V_{CEQ} = 320 \text{ mW}$$

Example-2 (Capacitor-Coupled CB Design)

Design a CB amplifier using an npn transistor as shown in **fig. 3** with $\beta = 100$, $V_{CC} = 24$ V, $R_{load} = 2K\Omega$, $R_E = 400\Omega$ $V_{BE} = 0.7$V. Design this amplifier for a voltage gain of 20.

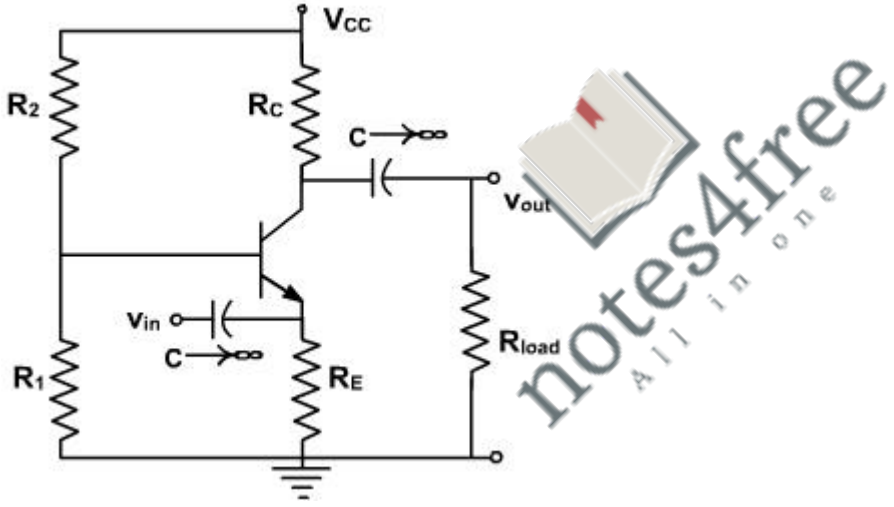


Fig. 3

Solution:

Since there are fewer equations than there are unknowns, we need an additional constraint, so we set

$R_C = R_{load} = 2$ K Ω

Then we have,

$$R_B + r'_E = \frac{R_{load} \,||\, R_C}{A_v} = 50 \ \Omega$$

R_{ac} = 1.40 K Ω and R_{dc} =2.40 KΩ

For maximum swing, we set I_{CQ} to

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}} = 6.30 \ mA$$

We now find that

$$r_E' = \frac{0.025}{I_C} = 3.97 \ \Omega$$

$$R_B = \beta\,(50 - 3.97) = 4.60 \ K\Omega$$

The current gain is given by

$$A_i = \frac{400}{400 + 50} \ \frac{2000}{2000 + 2000} = 0.44$$

and input impedance is given by

$$R_{in} = R_E \left\| \left(r_e + \frac{R_B}{\beta} \right) \right. = 44 \ \Omega$$

We use the bias equation to find the parameters of the input bias circuitry.

$$V_{BB} = V_{BE} + I_{CQ}\left(\frac{R_B}{\beta} + R_E \right) = 3.51 \, V$$

The bias resistors are then given by

$$R_1 = \frac{R_B}{1 - V_{BB}/V_{CC}} = 5.38 \ K\Omega$$

$$R_2 = \frac{R_B V_{CC}}{V_{BB}} = 31.4 \ K\Omega$$

The maximum peak-to-peak undistorted output voltage is

V_{out}(peak-peak) = 1.8 | I_{CQ} | (R_{load} || R_C) = 11.3 V

Power rating is an important consideration in selecting bias resistors since they must be capable of withstanding the maximum anticipated (worst case) power without overheating. Power considerations also affect transistor selection. Designers normally select components having the lowest power handling capability suitable for the design. Frequently, de-rating (i.e., providing a "safety margin" from derived values) is used to improve the reliability of a device. This is similar to using safety factors in the design of mechanical systems where the system is designed to withstand values that exceed the maximum.

Consider a common emitter amplifier circuit shown in **fig. 1**.

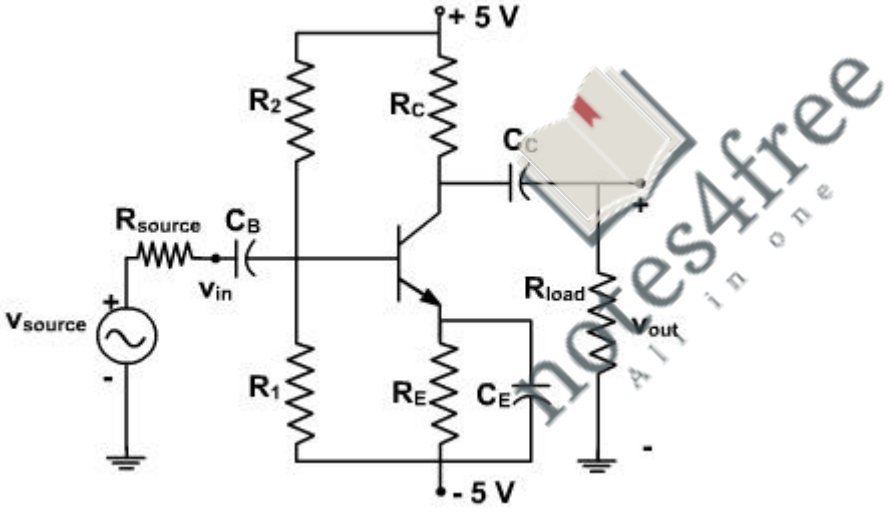


Fig. 1

Derivation of Power Equations

Average power is calculated as follows:

For dc: $$P = VI = I^2R = \frac{V^2}{R} \quad W \qquad \text{(E-1)}$$

For ac: $$P = \frac{1}{T}\int_0^T v(t).\, i(t)\, dt \quad W \qquad \text{(E-2)}$$

In the ac equation, we assume periodic waveforms where T is the period. If the signal is not periodic, we must let T approach infinity in equation E-1. Looking at the CE amplifier of **fig. 1**, the power supplied by the power source is dissipated either in R_1 and R_2 or in the transistor (and its associated collector and emitter circuitry). The power in R_1 and R_2 (the bias circuitry) is given by

$$R_{(bias)} = I^2_{R2} R_2 + I^2_{R1} R_1 \quad \text{(E-3)}$$

where I_{R1} and I_{R2} are the (downward) currents in the two resistors. Kirchhoff's current law (KCL) yields a relationship between these two currents and the base quiescent current.

$$I_{R1} = I_{R2} ? I_B \quad \text{(E-4)}$$

KVL yields the base loop equation (assuming $V_{EE} = 0$),

$$I_{R2} R_2 + I_{R1} R_1 = V_{CC} \quad \text{(E-5)}$$

These two equations can be solved for the currents to yield,

$$I_{R1} = \frac{V_{CC} - R_2 I_B}{R_2 + R_1}$$
$$I_{R2} = \frac{V_{CC} - R_1 I_B}{R_2 + R_1} \quad \text{(E-6)}$$

In most practical circuits, the power due to I_B is negligible relative to the power dissipated in the transistor and in R_1 and R_2. We will therefore assume that the power supplied by the source is approximately equal to the power dissipated in the transistor and in R_1 and R_2. This quantity is given by

$$P_{VCC} = \frac{1}{T}\int_0^T V_{CC}\left[I_{CQ} + i_c(t)\right] dt + P_{(bias\,circuit)} = V_{CC} I_{CQ} + \frac{V_{CC}^2}{R_1 + R_2} \quad \text{(E-7)}$$

Where the source voltage V_{CC} is a constant value. The source current has a dc quiescent component designated by i_{CEQ} and the ac component is designated by $i_c(t)$. The last equality of Equation (E-7) assumes that the average value of $i_c(t)$ is zero. This is a reasonable assumption. For example, it applies if the input ac signal is a sinusoidal waveform.

The average power dissipated by the transistor itself (not including any external circuitry) is

$$P(\text{transistor}) = \frac{1}{T}\int_0^T v_{CE}(t)\, i_C(t)\, dt \qquad \text{(E-8)}$$

For zero signal input, this becomes

$P(\text{transitor}) = V_{CEQ}\, I_{CQ}$

Where V_{CEQ} and I_{CQ} are the quiescent (dc) values of the voltage and current, respectively.

For an input signal with maximum possible swing (i.e., Q-point in middle and operating to cutoff and saturation),

$$v_{CE}(t) = V_{CEQ} - V_{CEQ} \sin \omega t = V_{CEQ}\,(1-\sin \omega t) \qquad \text{(E-9)}$$
$$i_c(t) = I_{CQ} + I_{CQ} \sin \omega t = I_{CQ}\,(1+\sin \omega t)$$
$$p(t) = v_{CE}(t) \cdot i_C(t) = \frac{V_{CEQ}\, I_{CQ}}{2}\,(1+\cos(2\omega t))$$

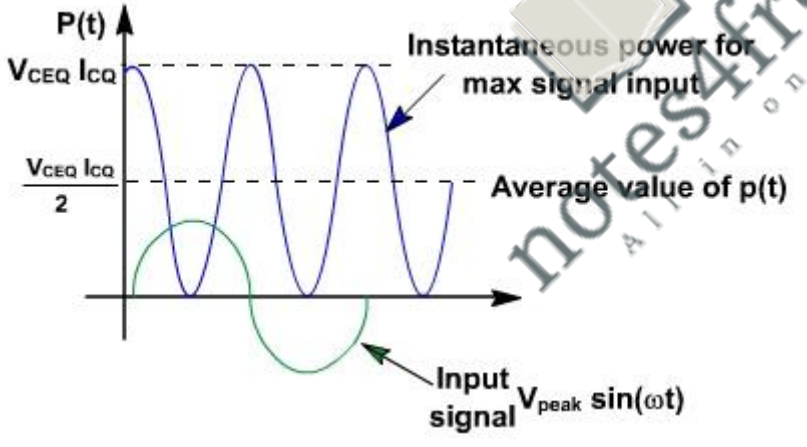


Fig. 2

Putting these time functions in Equation (E-7) yields the power equation,

$$P(\text{transistor}) = \frac{1}{T}\int_0^T V_{CEQ}\, I_{CQ}\left(1-\sin^2 \omega t\right)$$
$$= \frac{1}{T}\int_0^T V_{CEQ}\, I_{CQ}\left(\frac{1}{2}+\frac{1}{2}\cos 2\omega t\right)dt = \frac{V_{CEQ}\, I_{CQ}}{2} \qquad \text{(E-10)}$$

From the above derivation, we see that the transistor dissipates its maximum power (worst case) when no ac signal input is applied. This is shown in **fig. 2**, where we note that the frequency of the instantaneous power sinusoid is 2ω.

Depending on the amplitude of the input signal, the transistor will dissipate an average power between V_{CEQ} I_{CQ} and one half of this value. Therefore, the transistor is selected for zero input signal so it will handle the maximum (worst case) power dissipation of V_{CEQ} I_{CQ}.

We will need a measure of efficiency to determine how much of the power delivered by the source appears as signal power at the output. We define conversion efficiency as

$$\eta_{\text{conversion}} = \frac{P_{out(ac)}}{P_{in(dc)}} \times 100.$$

Cascade Amplifier:

To increases the voltage gain of the amplifier, multiple amplifier are connects in cascade. The output of one amplifier is the input to another stage. In this way the overall voltage gain can be increased, when number of amplifier stages are used in succession it is called a multistage amplifier or cascade amplifier. The load on the first amplifier is the input resistance of the second amplifier. The various stages need not have the same voltage and current gain. In practice, the earlier stages are often voltage amplifiers and the last one or two stages are current amplifiers. The voltage amplifier stages assure that the current stages have the proper input swing. The amount of gain in a stage is determined by the load on the amplifier stage, which is governed by the input resistance to the next stage. Therefore, in designing or analyzing multistage amplifier, we start at the output and proceed toward the input.

A n-stage amplifier can be represented by the block diagram as shown in **fig. 3**.

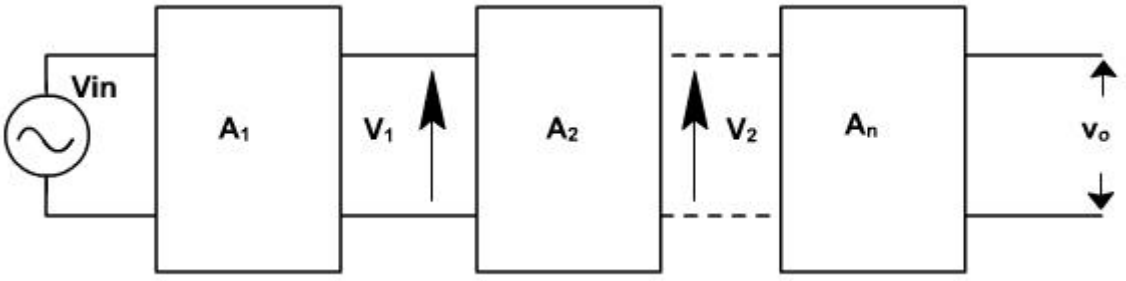


Fig. 3

In **fig. 3**, the overall voltage gain is the product of the voltage gain of each stage. That is, the overall voltage gain is ABC.

To represent the gain of the cascade amplifier, the voltage gains are represents in dB. The two power levels of input and output of an amplifier are compared on a logarithmic scale rather than linear scale. The number of bels by which the output power P_2 exceeds the input power P_1 is defined as

$$\text{No of bels} = \log_{10}\left(\frac{P_2}{P_1}\right)$$

$$\text{or No of dB} = 10 * \text{No. of bels}$$

$$= 10 \log_{10}\left(\frac{P_2}{P_1}\right)$$

Since,

$$P_1 = \frac{v_1^2}{R_{in}} \;\&\; P_2 = \frac{v_2^2}{R_0}$$

where R_{in} is the input resistance of the amplifier and R_0 is the load resistance

$$dB = 10 \log_{10}\left(\frac{v_2^2 / R_0}{v_1^2 / R_{in}}\right)$$

In case R_{in} and R_0 are equal, then power gain is given by

$$dB = 10 \log_{10}\left(\frac{v_2}{v_1}\right)^2 = 20 \log_{10}\left(\frac{v_2}{v_1}\right)$$

$$\therefore A_{dB} = A_{dB1} + A_{dB2} + \ldots\ldots$$

Because of dB scale the gain can be directly added when a number of stages are cascaded.

Types of Coupling:

In a multistage amplifier the output of one stage makes the input of the next stage. Normally a network is used between two stages so that a minimum loss of voltage occurs when the signal passes through this network to the next stage. Also the dc voltage at the output of one stage should not be permitted to go to the input of the next. Otherwise, the biasing of the next stage are disturbed.

The three couplings generally used are.

1. RC coupling
2. Impedance coupling
3. Transformer coupling.

1.RC coupling:

Fig. 4 shows RC coupling the most commonly used method of coupling from one stage to the next. An ac source with a source resistance R S drives the input of an amplifier. The grounded emitter stage amplifies the signal, which is then coupled to next CE stage the signal is further amplified to get larger output.

In this case the signal developed across the collector resistor of each stage is coupled into the base of the next stage. The cascaded stages amplify the signal and the overall gain equals the product of the individual gains.

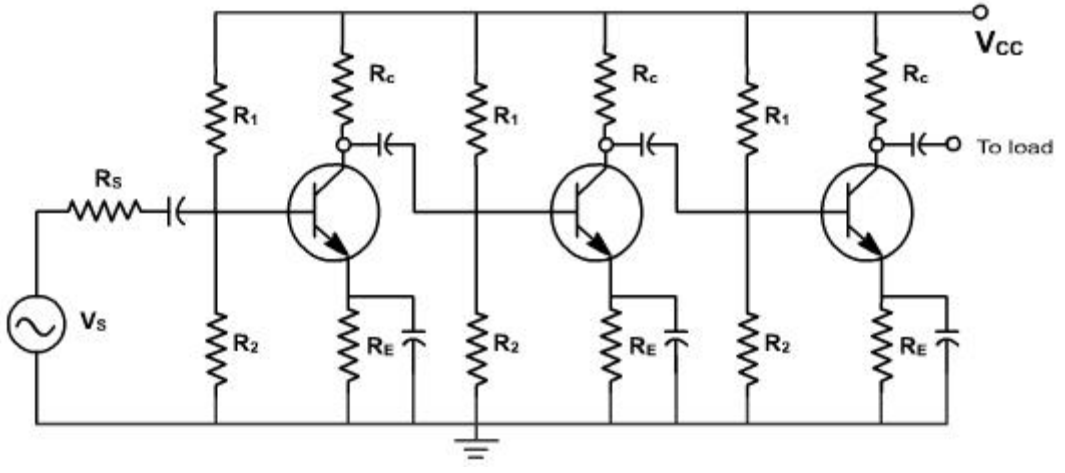


Fig. 4

The coupling capacitors pass ac but block dc Because of this the stages are isolated as for as dc is concerned. This is necessary to avoid shifting of Q-points. The drawback of this approach is the lower frequency limit imposed by the coupling capacitor.

The bypass capacitors are needed because they bypass the emitters to ground. Without them, the voltage gain of each stage would be lost. These bypass capacitors also place a lower limit on the frequency response. As the frequency keeps decreasing, a point is reached at which capacitors no longer look like a.c. shorts. At this frequency the voltage gain starts to decrease because of the local feedback and the overall gain of the amplifier drops significantly. These amplifiers are suitable for frequencies above 10 Hz.

Example - 1

Determine the current and voltage gains for the two-stage capacitor-coupled amplifier shown in **fig. 1**.

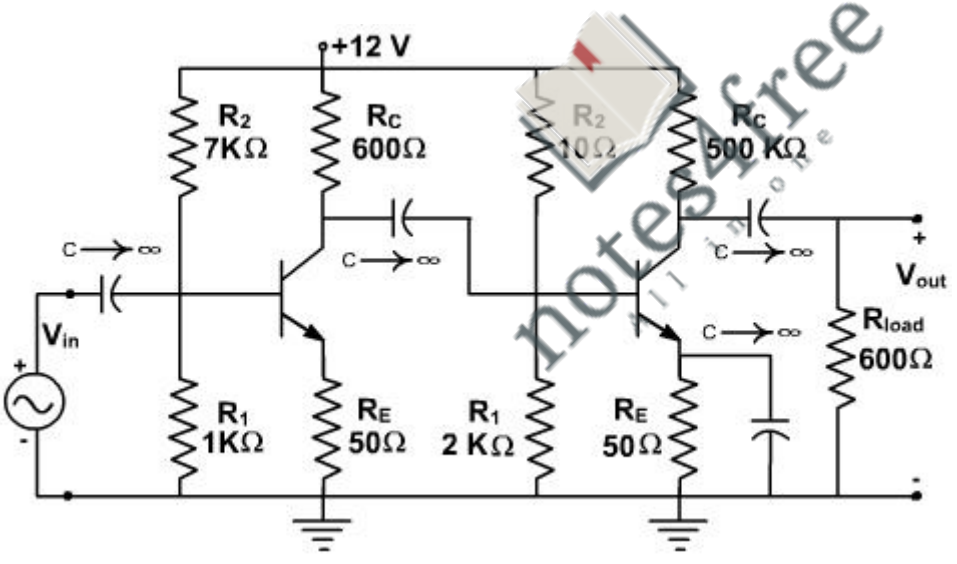


Fig. 1

Solution:

We develop the hybrid equivalent circuit for the multistage amplifier. This equivalent is shown in **fig. 2**. Primed variables denote output stage quantities and unprimed variables denote input stage quantities.

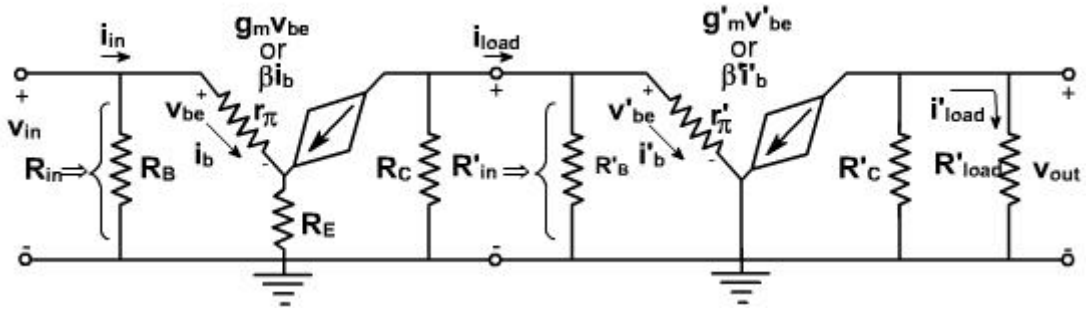


Fig. 2

Calculations for the output stages are as follows

$$R'_B = 10\,K\Omega \parallel 2\,K\Omega = \frac{10^4 \times 2 \times 10^3}{10^4 + 2 \times 10^3} = 1.67\,K\Omega$$

$$V'_{BB} = 12V \times \frac{2\,K\Omega}{10\,K\Omega + 2\,K\Omega} = \frac{12 \times 2 \times 10^3}{10^4 + 2 \times 10^3} = 2\,V$$

$$I'_{CQ} = \frac{V'_{BB} - V_{BE}}{R'_B/\beta + R'_B} = 22\,mA$$

$$r'_e = \frac{26(mV)}{I_{CQ}} = 1.77\ \ \Omega$$

For the input stage,

$$R_B = 7\,K\Omega \parallel 1K\Omega = \frac{7000 \times 1000}{7000 + 1000} = 875\,\Omega$$

$$V_{BB} = 12\,\frac{1K\Omega}{1\,K\Omega + 7\,K\Omega} = \frac{12 \times 1000}{700 + 1000} = 1.5\,V$$

$$I_{CQ} = \frac{1.5 - 0.7}{875/200 + 50} = 14.7\ \ mA$$

$$r_e' = \frac{26\ (mV)}{14.7\ (mA)} = 1.77\,\Omega$$

The input resistance is determined as:

$$R_{in} = R_B \| (r_\pi + \beta R_E) = \frac{875 \times 200 \times (1.77 + 50)}{875 + 10{,}354} = 807\ \Omega$$

The current gain, A_i, can be found by applying the equations derived earlier, where the first stage requires using the correct value for R_{load} derived form the value of R_{in} to the next stage.

Alternatively, we analyze **fig. 2** by extracting four current dividers as shown in **fig. 3**.

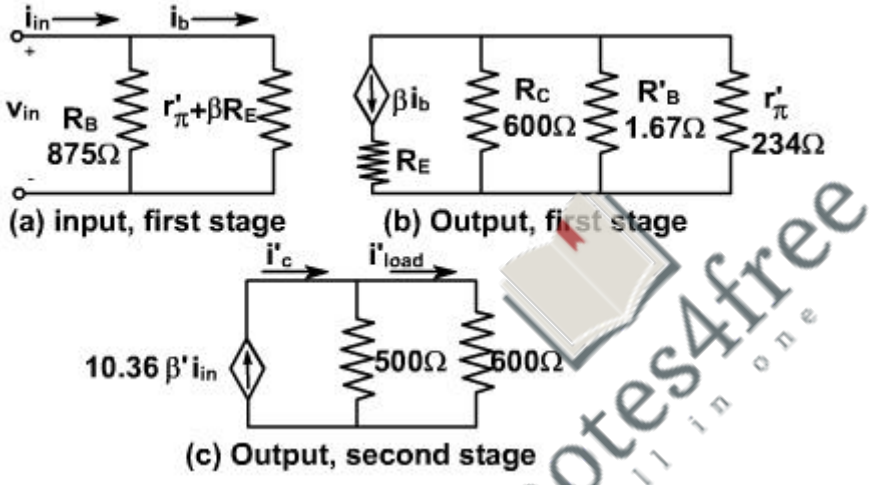


Fig. 3

The current division of the input stage is

$$i_b = \frac{R_B\, i_{in}}{R_B + r_\pi + \beta R_E} = 0.078\ i_{in}$$

The output of the first stage is coupled to the input of he second stage in **fig. 3(b)**. The input resistance of the second stage is

$$R'_{in} = R'_B \| r'_\pi = 205\ \Omega$$

The current in R'_{in} is i_{load} and is given by

$$i_{load} = \frac{15.6\, i_{in} \times 600}{805} = 11.6\, i_{in}$$

Again, i_{load} is current-divided at the input to the second stage. Thus,

$$i'_b = \frac{-R'_B\, i_{load}}{R'_B + r'_\pi} = -10.2\, i_{in}$$

The output current is found from **fig. 3(c)**:

$$i'_{load} = \frac{10.2\, i_{in} \times 200 \times 500}{500 + 600} = 927 \cdot i_{in}$$

The current gain is then

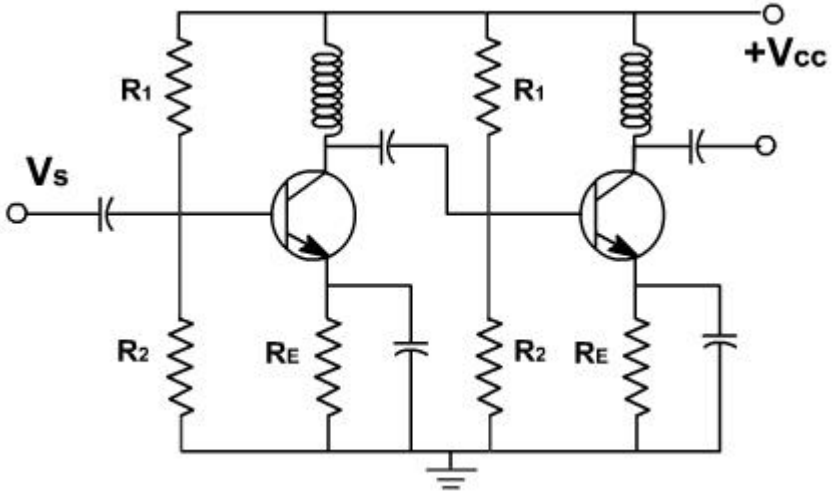
$A_i = 927$

Now using the gain impedance formula, we find the voltage gain:

$$A_v = \frac{927 \times 600}{807} = 689$$

Impedance Coupling:

At higher frequency impedance coupling is used. The collector resistance is replaced by an inductor as shown in **fig. 4**. As the frequency increases, X_L approaches infinity and each inductor appears open. In other words, inductors pass dc but block ac. When used in this way, the inductors are called RFchokes.



The advantage is that no signal power is wasted in collector resistors. These RF chokes are relatively expensive and their impedance drops off at lower frequencies. It is suitable at radio frequency above 20 KHz.

Transformer Coupling:

In this case a transformer is used to transfer the ac output voltage of the first stage to the input of the second stage. **Fig. 5**, the resistors R_C is replaced by the primary winding of the transformer. The secondary winding is used to give input to next stage. There is no coupling capacitor. The dc isolation between the two stages provided by the transformer itself. There is no power loss in primary winding because of low resistance.

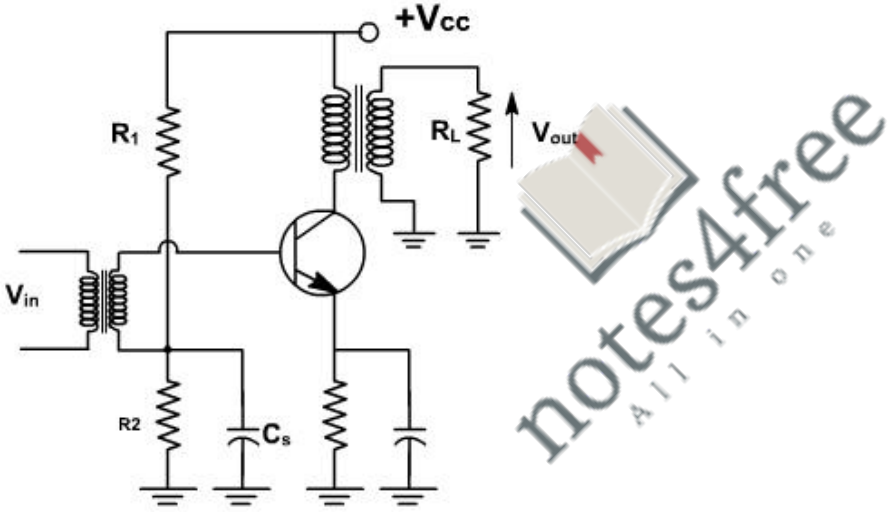


Fig. 5

At low frequency the size and cost of the transformer increases. Transformer coupling is still used in RF amplifiers. In AM radio receivers, RF signal have frequencies 550 to 1600 KHz. In TV receivers, the frequencies are 54 to 216 MHz. At these frequency the size and cost of the transformer reduces. C_S capacitor is used to make other point of transformer grounded, so that ac signal is applied between base and ground.

Tuned Transformer Coupling:

In this case a capacitor is shunted across primary winding to get resonance as shown in **fig. 6**. At this frequency the gain is maximum and at other frequencies the gain reduces very much.

This allows us to filter out all frequencies except the resonant frequency and those near it. This is the principle behind tuning in a radio station or TV channel.

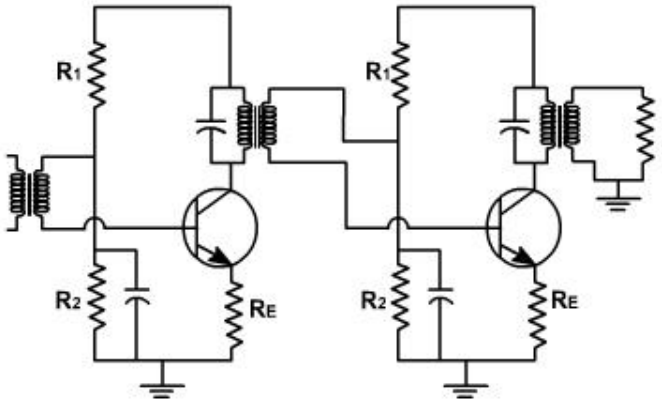


Fig. 6

Example - 2

Design a transformer-coupled amplifier as shown in **fig. 7** for a current gain of $A_i = 80$. Find the power supplied to the load and the power required from the supply.

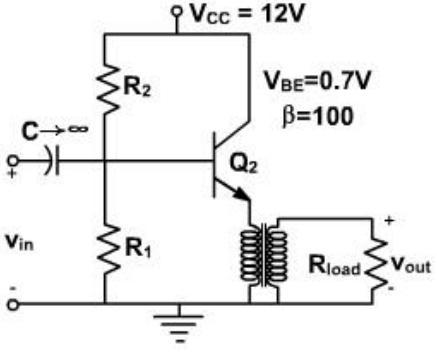


Fig. 7

Solution:

We first use the design equation to find the location of the Q-point for maximum output swing.

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}} = \frac{12}{a^2 R_{load}} = 23.4\text{mA}$$

Since the problem statement requires a current gain of 80, the amplifier must have a current gain of 10 because the transformer provides an additional gain of 8. We use the equations from Chapter 5 to find the base resistance R_B,

$$A_i = \frac{R_B}{R_B/\beta + r_e + R_E} = 10$$

where

$$R_E = a^2 R_{load} = 512\ \Omega$$

We note that r_e is sufficiently small to be neglected. Then, solving for R_B yields

$$R_B = 54.69\ K\Omega$$

$$V_{BB} = \frac{I_{CQ}R_B}{\beta} + V_{BE} = 2.03\ V$$

Now solving for the bias resistors,

$$R_1 = \frac{R_B}{1 + V_{BB}/V_{CC}} = 6.85\ K\Omega$$

$$R_2 = \frac{V_{CC}R_B}{V_{BB}} = 33.6\ K\Omega$$

The design is now complete. The power delivered by the source is given by

$$P_{V_{cc}} = V_{CC}I_{CQ} + \frac{V_{CC}^2}{R_1 + R_2} = 284\ mW$$

The power dissipated in the load is

$$P_{load} = \frac{(0.9a\, I_{CQ})^2\, R_{load}}{2} = 114\ \ mW$$

We have restricted operation to the linear region by eliminating 5% of the maximum swing near cutoff and saturation. The efficiency is the ratio of the load to source power.

$$\eta = \frac{114}{284} = 0.4 \text{ or } 40\ \%$$

Module-4

Power Amplifier

The amplifiers in multistage amplifier near the load end in almost all-electronic system employ large signal amplifiers (Power amplifiers) and the purpose of these amplifiers is to obtain power again.

Consider the case of radio receiver, the purpose of a radio receiver is to produce the transmitted programmes with sufficient loudness. Since the radio signal received at the receiver output is of very low power, therefore, power amplifiers are used to put sufficient power into the signal. But these amplifier need large voltage input.

Therefore, it is necessary to amplify the magnitude of input signal by means of small amplifiers to a level that is sufficient to drive the power amplifier stages.

In multistage amplifier, the emphasis is on power gain in amplifier near the load. In these amplifies, the collector currents are much larger because the load resistances are small (i.e impedence of loud speaker is 3.2 ohm).

A power amplifier draws a large amount of dc power form dc source and convert it into signal power. Thus, a power amplifier does not truly amplify the signal power but converts the dc power into signal power.

DC and AC load lines:

Consider a CE amplifier as shown in **fig. 1**.

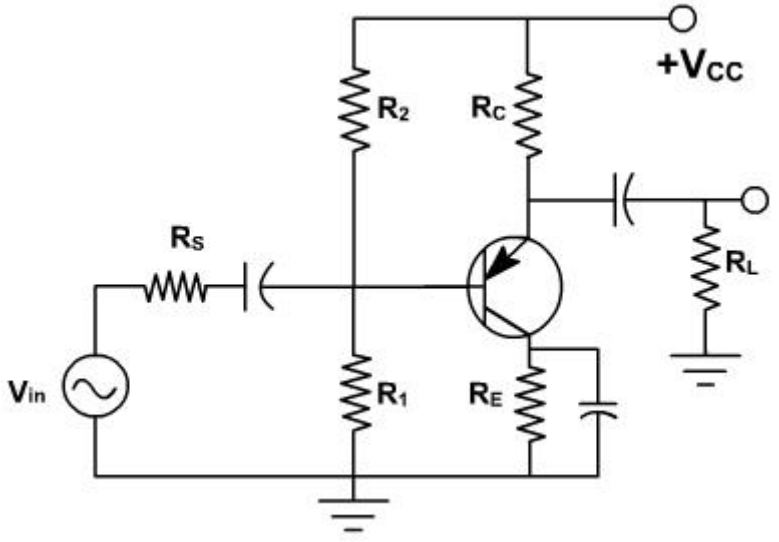


Fig. 1

The dc equivalent circuit gives the dc load line as shown in **fig. 2**.

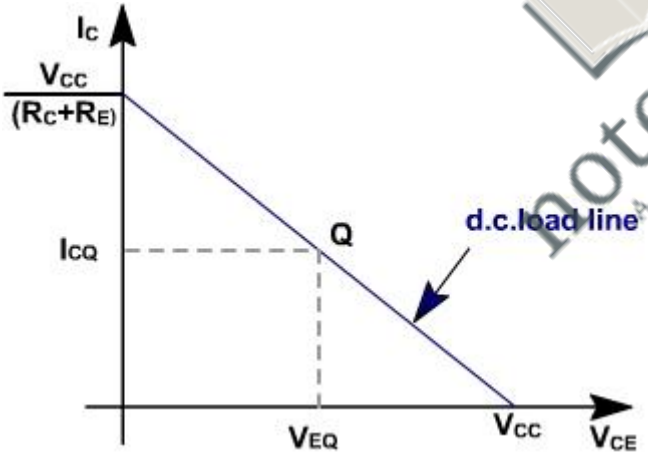


Fig. 2

Q is the operative point. I_{CQ} and V_{CEQ} are quiescent current and voltage. The ac equivalent circuit is shown in **fig. 3**.

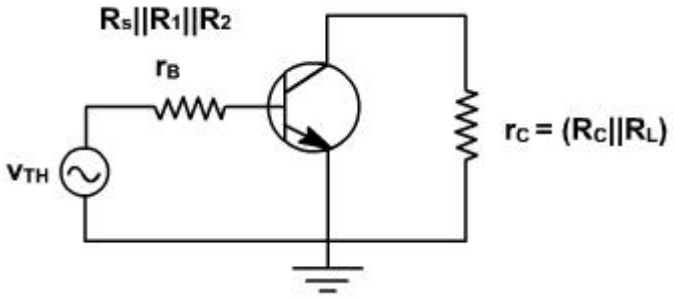


Fig. 3

This circuit produces ac load line. When no signal is present, the transistor operates at the Q point shown in **fig. 4**.

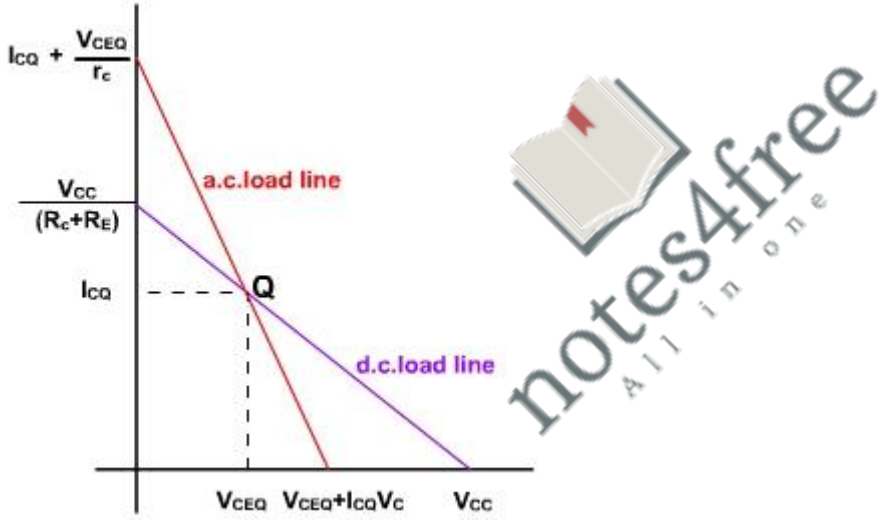


Fig. 4

When a signal is present, operating point swings along the ac load line rather than dc load line. The saturation and cut off points on the ac load line are different from those on the dc load line.

$$V_{ce} + i_c r_c = 0$$

or

$$i_c = -\frac{V_{ce}}{r_c}$$

The ac collector current is given by

$$i_c = I_C - I_{CQ}$$

$$V_{ce} = V_{CE} = V_{CE} - V_{CEQ}$$

$$I_C = I_{CQ} + \frac{V_{CEQ}}{r_c} + \frac{V_{CE}}{r_c}$$

when, $V_{CE} = 0$, $I_C = I_{CQ} + \frac{V_{CEQ}}{r_c}$

when, $I_C = 0$, $V_{CE} = V_{CEQ} + r_c I_{CQ}$

During the positive half cycle of ac source, voltage, the collector voltage swing from the Q-point towards saturation. On the negative cycle, the collector voltage swings from Q-point towards cutoff. For a large signal clipping can occur on either side or both sides.

The maximum positive swing from the Q-point is

$V_{CEQ} + I_{CQ} r_C$ ⇒ $V_{CEQ} = I_{CQ} r_C$.

The maximum negative swing from the Q-point is

0 ⇒ $V_{CEQ} = - V_{CEQ}$.

The ac output compliance (maximum peak to peak unclipped voltage) is given by the smaller of these two approximate values:

$PP = 2 I_{CQ} r_C$

or $PP = 2 V_{CEQ}$.

Class A operation:

In a class ‘A' operation transistor operates in active region at all times. This implies that collector current flows for 360° of the ac cycle.

Voltage gain of loaded amplifier

$$A_V = \frac{r_c}{r'_e}$$

Current gain

$$A_i = \frac{i_c}{i_b} = \beta$$

ac input power to the base $P_{in} = V_{in}\, i_b$

ac output power point = $- V_{out} * i_C$. (Negative sign is due to phase inversion.)

$$A_p = \frac{P_{out}}{P_{in}} = \frac{V_{out}}{V_{in}} * \frac{i_C}{i_b}$$

$$A_p = -A_v A_i$$

The ac power into a load resistor R_L is

$$P_L = \frac{V_L^2}{R_L}$$

Where V_L = rms load voltage

$$\therefore V_L = 0.707\, V_p$$

$$V_p = \frac{V_{PP}}{2}$$

$$\therefore P_L = \left(\frac{0.707 * V_{PP}}{2}\right) * \frac{1}{R_L}$$

$$= \frac{V_{PP}^2}{8R_L}$$

The variation of P_L with V_{PP} is shown in **fig. 5**. Maximum ac load power is obtained when the output unclipped voltage equals ac output compliance PP.

$$\therefore P_{L(max)} = \frac{PP^2}{8R_L}$$

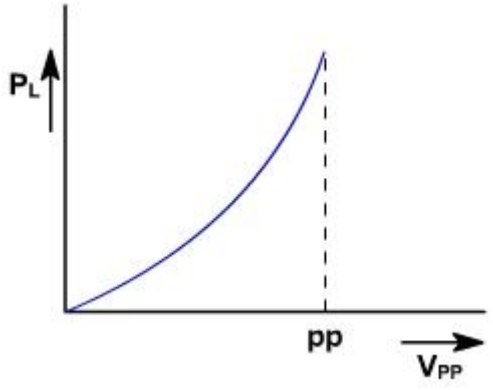


Fig. 5

When no signal drives the amplifier, the power dissipation of the transistor equals the product of d. voltage and current

$P_{DQ} = V_{CEQ} * I_{CQ}$

When there is no input signal, P_D is maximum as shown in **fig. 6**.

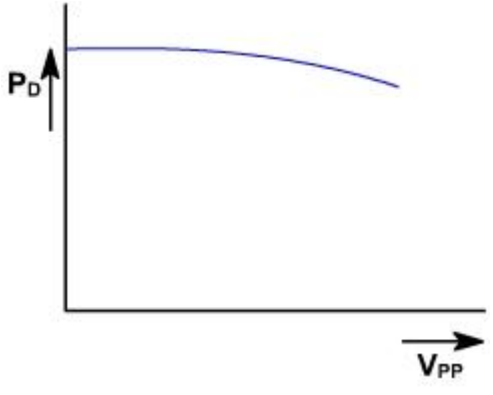


Fig. 6

It decreases when the peak to peak load voltage increases. The power dissipation must be less than the rating of transistor, otherwise temperature increases and transistor may damage. To reduce the temperature, heat sinks are used that dissipates the heat produced. When Q-point is at the center of ac load line then peak swing above and below Q-point is equal.

$$V_P = V_{CEQ} = i_{CQ} * r_C$$

$$\therefore P_D = \frac{V_P^2}{2 * r_C}$$

$$= \frac{V_{CEQ} * I_{CQ} * r_C}{2 * r_C}$$

$$= \frac{V_{CEQ} * I_{CQ}}{2}$$

$$= \frac{P_{DQ}}{2}$$

Class A current drain:

In a class A amplifier shown in **fig.1**, the dc source V_{CC} must supply direct current to the voltage divider and the collector circuit.

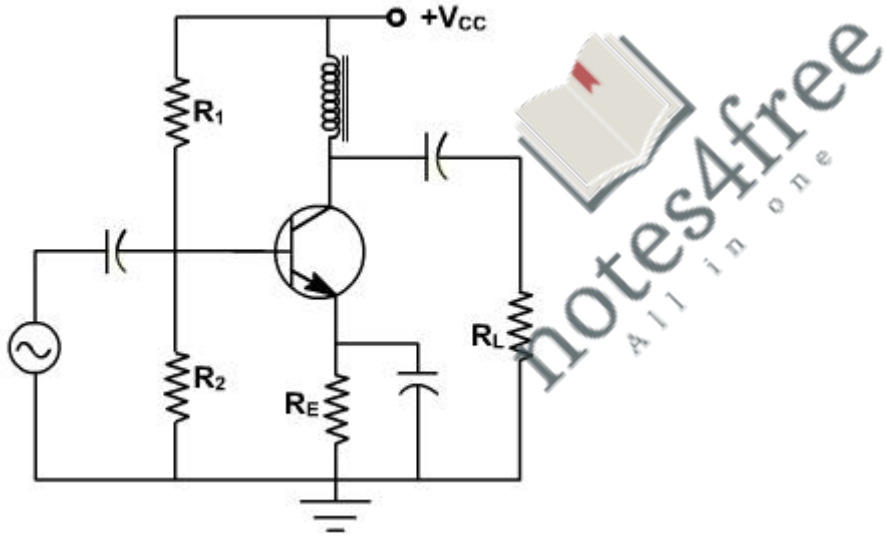


Fig. 1

Assuming a stiff voltage divider circuit, the dc current drain of the voltage divider circuit is

$I_1 = V_{CC} / (R_1 + R_2)$

In the collector circuit, the dc current drain is

$I_2 = I_{CQ}$

In a class A amplifier, the sinusoidal variations in collector current averages to zero. Therefore, whether the ac signal is present or not, the dc source must supply an average current of

$I_S = I_1 + I_2$.

This is the total dc current drain. The dc source voltage multiplied by the dc current drain gives the ac power supplied to an amplifier.

$P_S = V_{CC} I_S$

Therefore, efficiency of the amplifier, $\eta = (P_{L(max)} / P_S) * 100\ \%$

Where,, $P_{L(max)}$ = maximum ac load line power. In class A amplifier, there is a wastage of power in resistor R_C and R_E i.e. $I_{CQ}^2 * (R_C + R_E)$.

To reduce this wastage of power R_C and R_E should be made zero. R_E cannot be made zero because this will give rise to bias stability problem. R_C can also not be made zero because effective load resistance gets shorted. This results in more current and no power transfer to the load R_L. The R_C resistance can, however, be replaced by an inductance whose dc resistance is zero and there is no dc voltage drop across the choke as shown in **fig. 1**.

Since in most application the load is loudspeaker, therefore power amplifier drives the loudspeaker, and the maximum power transfer takes place only when load impedence is equal to the source impedence. If it is not, the loud speaker gets less power. The impedence matching is done with the help of transformer, as shown in **fig. 2**.

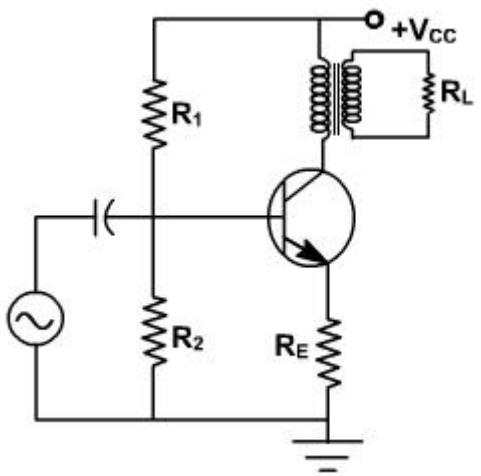


Fig. 2

The ratio of number of turns is so selected that the impedence referred to primary side can be matched with the output impedence of the amplifier.

$$\frac{R_L'}{R_L} = \frac{V_1/I_1}{V_2/I_2} = \left(\frac{V_1}{V_2}\right)\left(\frac{I_2}{I_1}\right) = \left(\frac{N_1}{N_2}\right)^2$$

$$\therefore R_L' = R_L\left(\frac{N_1}{N_2}\right)^2$$

Class B amplifier:

The efficiency (□) of class A amplifier is poor. The reason is that these circuits draw considerable current from the supply even in the absence of input signals.

In class B operation the transistor collector current flows for only 180° of the ac cycle. This implies that the Q-point is located approximately at cutoff on both dc and ac load lines. The advantages of class B operation are

- Lower transistor power dissipation
- Reduced current drain.
- Eficiency is given by

$$\eta_{(max)} = \frac{P_{ac}}{P_{dc}} = \frac{2V_{CC}\,2I_C}{8V_{CC}I_C} \times 100\%$$

- Value is around 70%

Push pull circuit:

When a transistor operates in class B, it clips off a half cycle. To avoid the resulting distortion, two transistors are used in push pull arrangement. This means that one transistor conducts during positive half cycle and other

Fig. 3

transistor conducts during negative half cycle. The distortion is low, load power is large and efficiency (□ □) is more. **fig. 3**, shows how a npn and pnp transistor emitter followers are connected in push pull arrangement.

The dc & ac equivalent circuit are shown in **fig. 4** & **fig. 5**. The biasing resistors are selected so that Q-point is set at cutoff. This biases the emitter diode of each transistor between 0.6V and 0.7V

i.e. $I_{CQ} = 0$.

Because the biasing resistors are equal each emitter diode is biased with the same voltage. As a result half the supply voltage is dropped across each transistor.

$V_{CEQ} = V_{CC} / 2$.

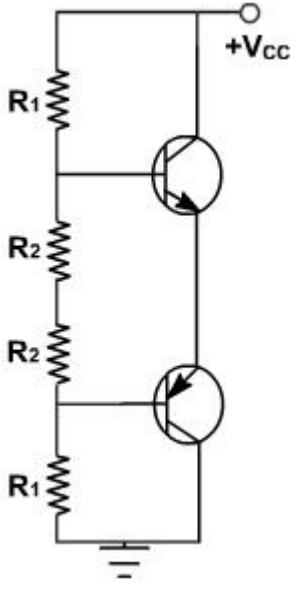


Fig. 4

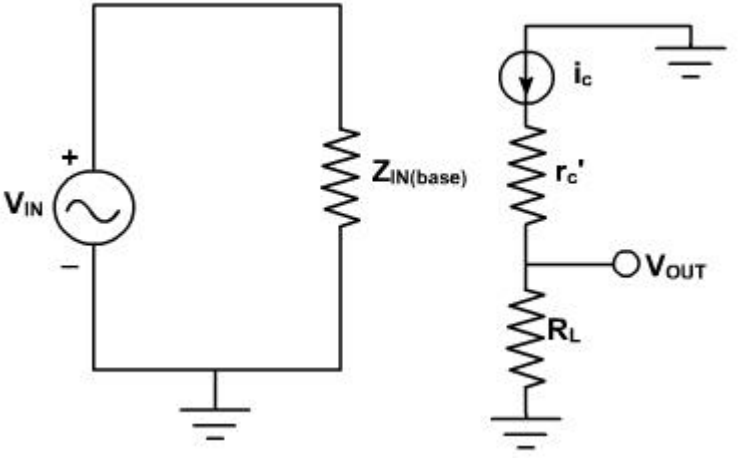


Fig. 5

Since there is no dc resistance in the collector or emitter circuits, the dc saturation current is infinite. The dc load line is vertical as shown in **fig. 6**. The most difficult thing is setting up a stable Q-point at cut off. Any significant increase in V_{BE} with temperature can move the Q-point up the dc load line to dangerously high currents. Ac load line is given by

$I_{C(sat)} = I_{CQ} + (V_{CEQ} / r_E)$

$V_{CE\ (cut\ off)} = V_{CEQ} + I_{CQ}\, r_E$

$I_{CQ} = 0$; $V_{CEQ} = V_{CC} / 2$

i.e. $I_{C(sat)} = V_{CC} / 2R_L$ (i.e. $r_E = R_L$)

$V_{CE\ (cut\ off)} = V_{CC} / 2.$

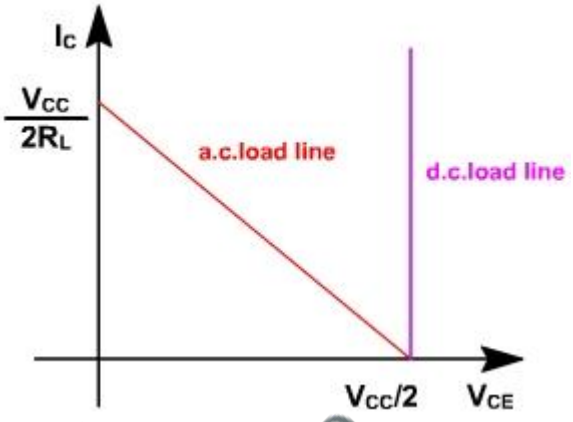


Fig. 6

When either transistor is conducting, that transistor's operating point swings along the ac load line and the operating point of the other transistor remains at cut off. The voltage swing of the conducting transistor can go from cut off to saturation. In the next half cycle, the other transistor does the same thing.

Therefore, $PP = V_{CC}$

Voltage gain of loaded amplifier:

$A_V = R_L / (R_L + r'_e)$

$Z_{in\ (base)}$ □ □ □$(R_L + r'_e)$

$Z_{out} = r'_e + (r_B) /$□ □

$A_P = A_V * A_i$

Without signal the capacitor charges up to $V_{CC} / 2$ relative to ground.

In the positive half cycle of input voltage, the upper transistor conducts and the lower one cut off. The upper transistor acts like an ordinary emitter follower, so that the output voltage

approximately equals the input voltage. The current flow through R_L is such as direct as to make output positive.

In the negative half cycle of input voltage, the upper transistor cuts off and the lower transistor conducts. The lower transistor acts like an ordinary emitter follower and produces a load voltage approximately equal to the input voltage (i.e. negative output. Since Q, is off, no current can flow from V_{CC} through Q, but capacitor acts like a battery source and discharges).

During either half cycle, the source sees a high input impedence looking into either base and the load sees a low output impedence.

Cross over distortion:

Fig. 1 shows the ac equivalent circuit of a class B push pull amplifier. Suppose that no bias is applied to the emitter diodes. Then the incoming voltage has to rise to about 0.7 V to overcome the barrier potential. Because of this no current flows through Q, when the signal is less than 0.7 V. The action is similar on the other half cycle no current flows in Q_2 until ac voltage is more negative the – 0.7 V. If no bias is applied the output of class B amplifier looks like as shown in **fig. 1.**

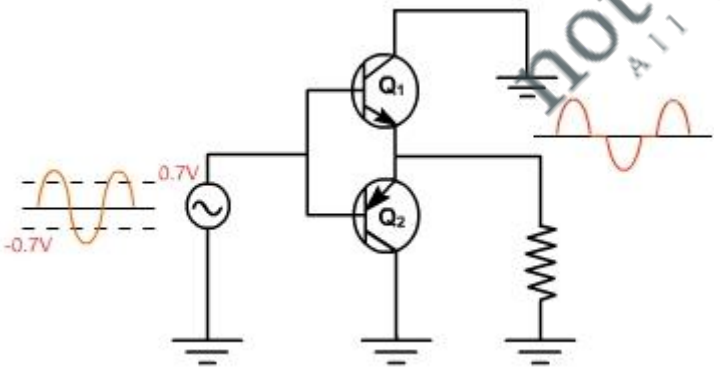


Fig. 1

The signal output is distorted. Because of clipping action between half cycles, it no longer is a sine wave. Since the clipping occurs between the time one transistor cuts off and the time the other comes on, it is called cross over distortion. To eliminate cross over distortion, the slight forward bias must be applied to each emitter diode. This means locating the Q-point

slightly above cut off as shown in **fig. 2**. In fact, this is class AB operation. This means that collector current flows for more than 180 degrees but less than 360°.

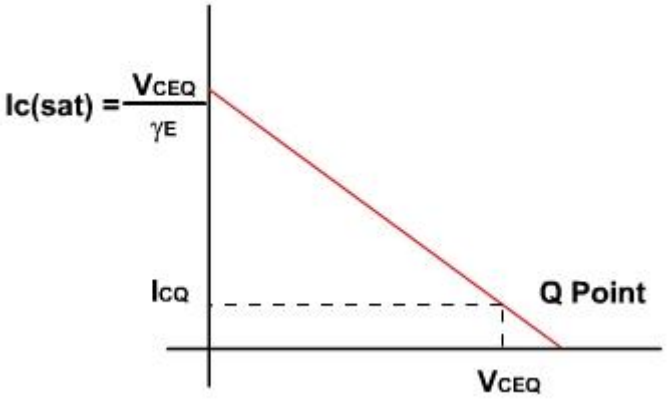


Fig. 2

Class A amplifier introduces non-linear distortion in input wave means elongates one half cycle and compresses one half cycle. This can be reduced by swamping. In this case it can be further reduced because both half cycles are identical in shape, is given by non-linear distortion is much less than class A.

Load power is given by

$$P_L = \frac{V_{PP}^2}{8R_L}$$

Since the ac output compliance equals the peak-to-peak voltage, the maximum load power is

$$P_{L(max)} = \frac{V_{CC}^2}{8R_L}$$

$$= \frac{V_{CEQ}^2}{2R_L}$$

$$\text{Current drain } I_s = I_1 + I_2$$

Where, I_1 = current through biasing resistance. When no signal is present $I_2 = I_{CQ}$ and the current drain is small. But when a signal is present, the current drain increase because the upper collector current becomes large.

If the entire ac load line is used, then the upper transistor has a half sine wave of current through it with a peak value of

$I_{C(sat)} = V_{CEQ} / R_L$

The average value of half sine wave is given by

$$I_2 = \frac{1}{2\pi}\int_0^{\pi}\frac{V_{CEQ}}{R_L}\sin\omega t.d\,\omega t$$
$$= \frac{V_{CEQ}}{R_L} * \frac{1}{\pi}$$
$$= \frac{0.318 V_{CEQ}}{R_L}$$

The dc power is supplied to the circuit is $P_S = V_{CC}$ is under no signal conditions, the dc power is small because the current drain is minimum. But when a signal uses the entire ac load line, the dc power supplied to the circuit reaches a maximum.

Biasing a class B amplifier:

In class B amplifier, two complement any transistors are required. Because of the series connection, each transistor drops half the supply voltage. To avoid cross over distortion, the Q-point slightly above cut off, with the correct V_{BE} somewhere between 0.6 and 0.7.

If there is an increase in V_{BE} by few mV it produces 10 times as much emitter current. Because of this it is difficult to find standard resistors that can produce the correct V_{BE} and it needs an adjustable resistor.

The biasing does not solve thermal instability problem. Because for a given collector current, V_{BE} requirement decreases by 2 mV per degree rise in temperature. The voltage divider produces a stiff drive for each diode. Therefore as the temperature increases, the fixed voltage on each emitter diode forces the collector current to increase and this gives rise to thermal run away. When the temperature increases collector current increases, and this is equivalent to Q-point moving up along the vertical dc load line. As the Q-point moves toward higher collector currents, the temperature of the transistor increases further reducing the required V_{BE} .

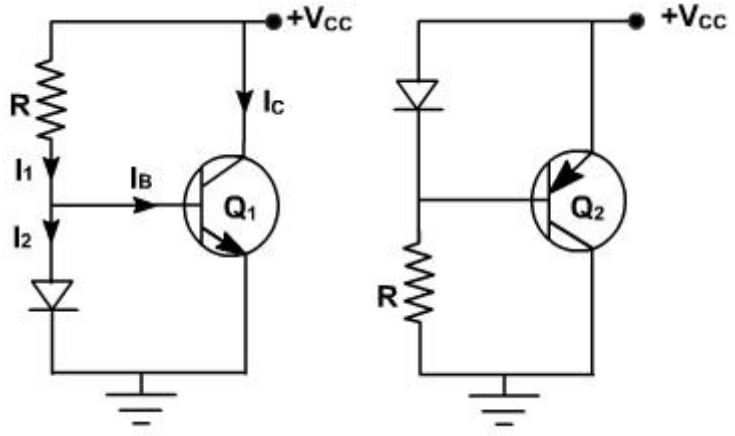


Fig. 3

One way to avoid thermal run away is to use diode bias. It is based on the concept of current mirror as shown in **fig. 3**, the base current is much smaller than the current through the resistor and diode. For this reason, I_1 and I_2 are approximately equal. If the diode curve is identical to the V_{BE} curve of the transistor (V_{BE}, I_E). The diode current equals the emitter and also collector current. Therefore I_1 is nearly equal to I_C.

$I_1 = I_C$.

The collector current is set by controlling the resistor current. This is called a current mirror.

Similarly, pnp transistor can be used as a current mirror. If the V_{BE} curve of the transistor matches the diode curve, the collector equals the resistor current.

Diode bias of class B push pull emitter follower relies on two current mirrors as shown in **fig. 4**.

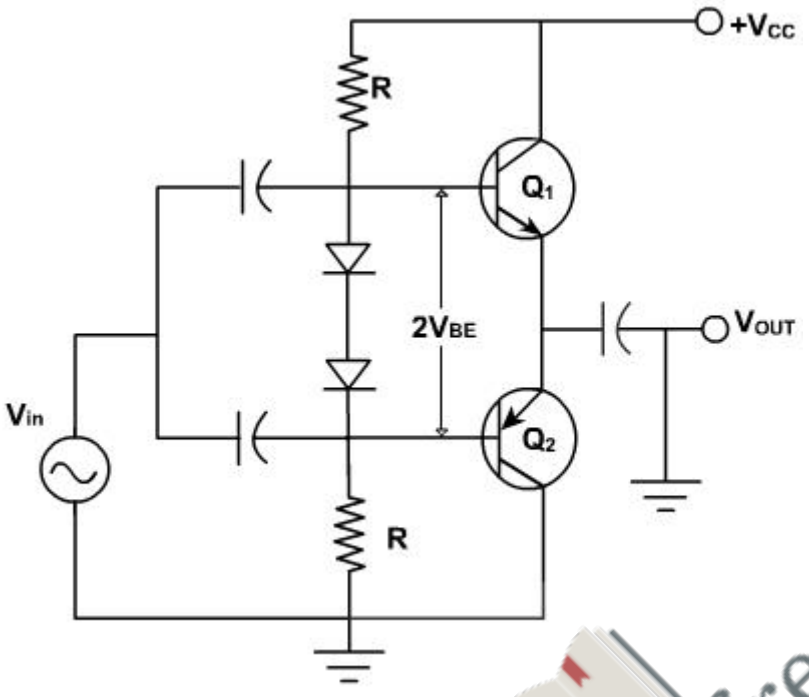


Fig. 4

The upper half is an npn current mirror, and the lower half is a pnp current mirror as shown in **fig. 4**. For diode bias to be immune to changes in temperature, the diode curve must match the V_{BE} curves of the transistor over a wide temperature range. This is easily done in ICs .

Power Calculations for Class B Push-Pull Amplifier

The power delivered by the ac source is split between the transistor and the resistors in the bias circuitry. The ac signal source adds an insignificant additional amunt of power since base currents are small relative to collector currents. Part of the power to the transistor goes to load, and the other part is dissipated by the transistor itself. The following equations specify the various power relationships in the circuit.

The average power supplied by the dc source is

$$P_{VCC} = V_{CC} I_{DC} = V_{CC} \frac{1}{T} \int_0^T i_{cc}(t)dt$$

$i_{CC}(t)$ is the total current and is composed of two components: the dc current through the base bias resistor and diode combination, and the ac collector current through transistor, Q_1. Under quiescent conditions (i.e. zero input) Q_1 is in cutoff mode. Collector current flows during the positive half of the output signal waveform. Therefore we only need to integrate this component of the power supply signal over the first half cycle.

$$I_{C1avg} = \frac{1}{T}\int_0^{T/2} I_{Cmax}\sin\left(\frac{2\pi t}{T}\right)dt = \frac{1}{\pi} I_{C1max}$$

The maximum values of collector current and power delivered to the transistor are

$$I_{Cmax} = \frac{V_{CC}}{2R_{load}}$$

$$P_{VCC}\big|_{Q1,Q2} = \frac{V_{CC} I_{Cmax}}{\pi} = \frac{V_{CC}^2}{2\pi R_{load}}$$

The ac output power, assuming a sinusoidal input, is

$$P_{out}(ac) = \frac{I_{Cmax}^2 R_{load}}{2}$$

The maximum ac output power is found by substituting I_{Cmax} for I_{C1max} to get

$$P_{out}(acmax) = \frac{1}{2}\left(\frac{V_{CC}}{2R_{load}}\right)^2 R_{load} = \frac{V_{CC}^2}{8R_{load}}$$

The total power supplied to the stage is the sum of the power to the transistor and the power to the bias and compensation circuitry.

$$P_{VCC} = \frac{V_{CC}\, I_{Cmax}}{\pi} + \frac{V_{CC}^2}{2R_f + 2R_2}$$

If we subtract the power to the load from the power supplied to the transistors, we find the power being dissipated in the transistors the power dissipated by a single transistor is one half of this value. Thus,

$$P_{transistor} = \frac{1}{2}\left(\frac{V_{CC}\, I_{Cmax}}{\pi} - \frac{I_{Cmax}^2 R_{load}}{2}\right)$$

we are assuming that the base current is negligible. The efficiency of the Class B push-pull amplifier is the ratio of the output power to the power delivered to the transistor. Thus we neglect the power dissipated by the bias circuitry.

$$\eta = \frac{V_{CC}^2 / 8 R_{load}}{V_{CC}^2 / 2\pi R_{load}} = \frac{\pi}{4} = 0.785 \text{ or } 78.5\%$$

This amplifier is more efficient than a Class A amplifier. It is often used in output circuits where efficiency important design requirement.

$$\frac{dP}{dI_{Cmax}} = 0 = \frac{1}{2}\left(\frac{V_{CC}}{\pi} - I_{Cmax}R_{load}\right)$$

$$I_{C1max} = \frac{V_{CC}}{\pi R_{load}}$$

Therefore, $$Pmax = \frac{1}{2}\left(\frac{V_{CC}^2}{\pi^2 R_{load}} - \frac{V_{CC}^2}{2\pi^2 R_{load}}\right) = \frac{V_{CC}^2}{4\pi^2 R_{load}}$$

In choosing a transistor, it is important that the power rating is equal to or exceeds the maximum power P_{max}.

Class C amplifier:

A class C amplifier can produce more power than a class B amplifier.

Consider the case of a radio transmitter in which the audio signals are raised in their frequency to the medium or short wave band to that they can be easily transmitted. The high frequency introduced is in radio frequency range and it serves as the carrier of the audio signal. The process of raising the audio signal to radio frequency called modulation.

The modulated wave has a relatively narrow band of frequencies centered around the carrier frequencies. At any instant, there are several transmitter transmitting programmes simultaneously. The radio receiver selects the signals of desired frequencies to which it is tuned, amplifies it and converts it back to audio range. Therefore, tuned voltage amplifiers are used. In short, the tuned voltage amplifiers selects the desired radio frequency signal out of a number of RF signals present at that instant and then amplifies the selected RF signal to the desired level as shown in **fig. 1**.

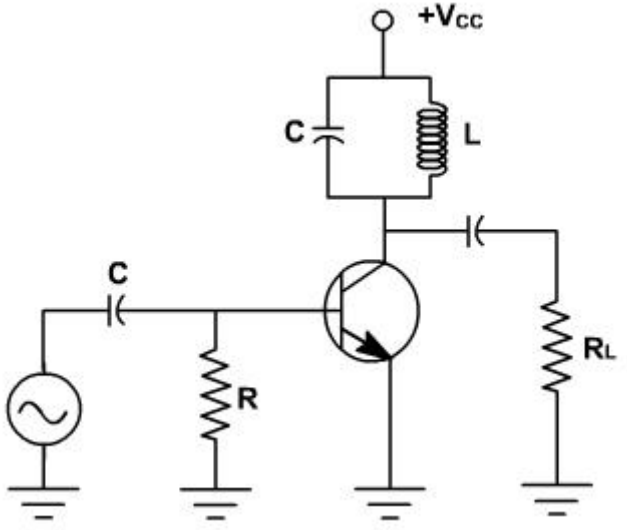


Fig. 1

Class C operation means that the collector current flows for less than 180° of the ac cycle. This implies that the collector current of a class C amplifier is highly non-sinusoidal because current flows in pulses. To avoid distortion, class C amplifier makes use of a resonant tank circuit. This results in a sinusoidal output voltage.

The resonant tank circuit is tuned to the frequency of the input signal. When the circuit has a high quality factor (Q) parallel resonance occurs at approximately

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

At the resonance frequency, the impedence of the parallel resonant circuit is very high as shown in **fig. 2** and is purely resistive. When the circuit is tuned to the resonant frequency, the voltage across R_L is maximum and sinusoidal. The higher the Q of the circuit, the faster the gain drops off on either side of resonance

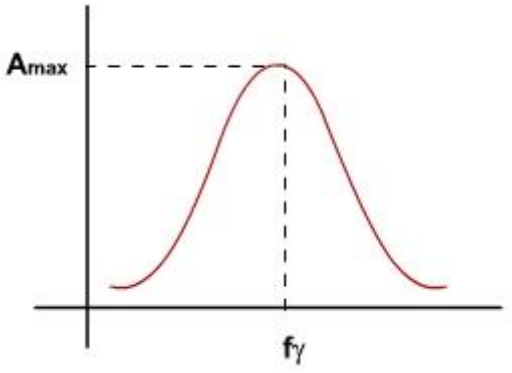


Fig. 2

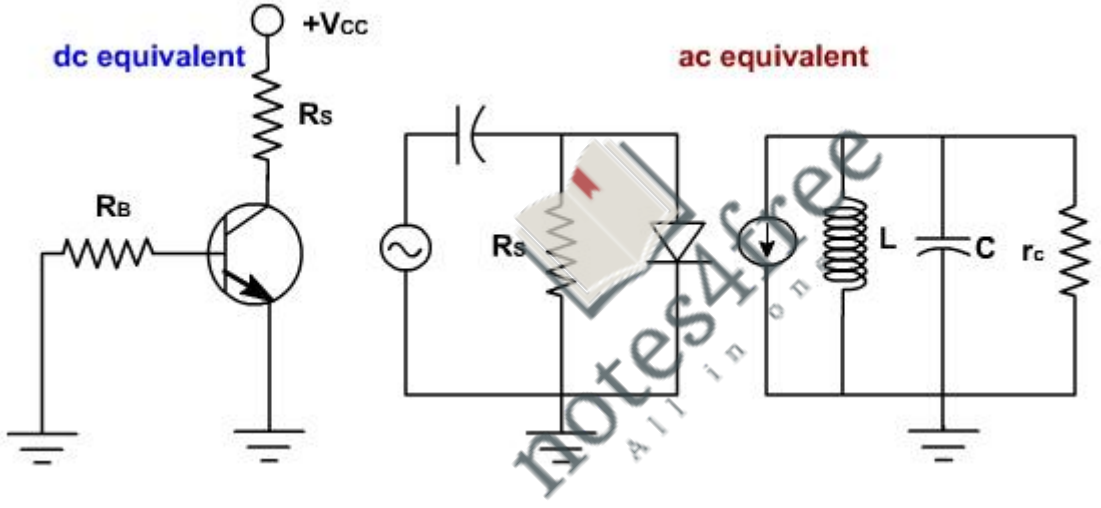


Fig. 3

The dc equivalent circuit is shown **fig. 3**. No bias is applied to the transistor. Therefore, its Q-point is at cut off on the dc load line V_{BE}= 0.7V. Therefore no I_L current flows until input is more than 0.7 V. Also dc resistance is R_S (the resistance of inductor) which is very small and therefore dc load line is almost vertical. There is no danger of thermal runway because there is no current other than from leakage.

The $I_{C(sat)}$ current is given by

$$I_{C(sat)} = I_{CQ} + \frac{V_{CEQ}}{r_C}$$

where r_C is the collector resistance.

The voltage VCE(sate) is given by

$$V_{CE(sat)} = V_{CEQ} + I_{CQ}\, r_C$$

when $I_{CQ} = 0$, $V_{CEQ} = V_{CC}$

$$\therefore I_{C(sat)} = \frac{V_{CC}}{r_C}$$

and $V_{CE(sat)} = V_{CC}$

When the Q of a resonant circuit is greater than 10. One can use the approximate ac equivalent circuit. The series resistance of the inductor is lumped into the collector resistance. At resonance, the peak-to-peak load voltage reaches a maximum. The bandwidth of a resonant circuit is given by

Band width (BW) = f_2 – f_1

f_1 = Lower cut off frequency.

f_2 = Upper cut off frequency

The bandwidth is related to the resonant frequency and the circuit Q as below:

$BW = f_r / Q$

This means a large Q produces small BW equivalent to sharp tuning. These amplifiers have Q greater than 10. This means that the BW is less than 10% of the resonant frequencies. These amplifiers are also called narrow band amplifier.

When the tank circuit is resonant the ac load impedence seen by the collector current source is purely resistive and the collector current is minimum. Above and below resonance, the ac load impedence decreases and the collector current decreases. Any coil or inductor has some series resistance R_S as shown in **fig. 4**.

The Q of all coil is given by.

$Q_L = X_L / R_L$

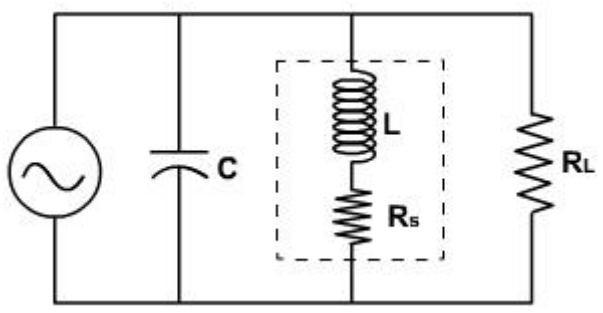


Fig. 4

The series resistance can be replaced by parallel resistance R_P . This equivalent resistance is given by

$R_P = Q_L R_L$

Now all the losses in the coil are now being represented by the parallel resistance R_P and series resistance R_S no longer exists X_C cancels X_L at resonance. Leaving only R_P in parallel with R_L.

Therefore,

$R_C = R_P \parallel R_L$

Q of the overall circuit = r_C / X_L

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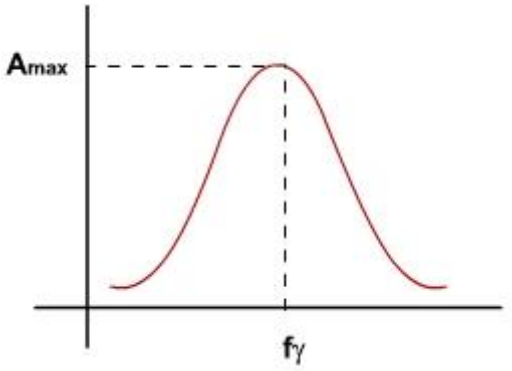

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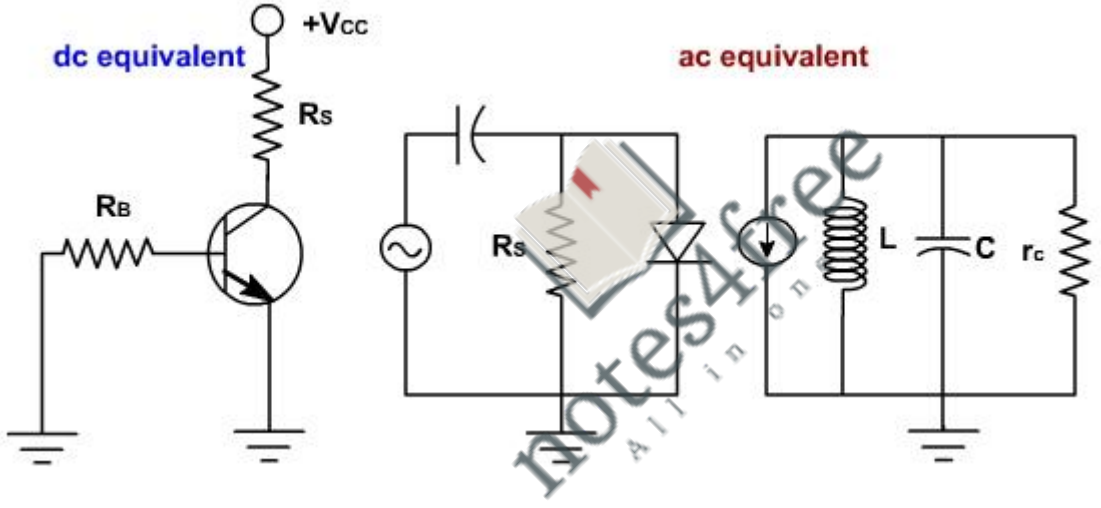

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and $V_{CE(sat)} = V_{CC}$

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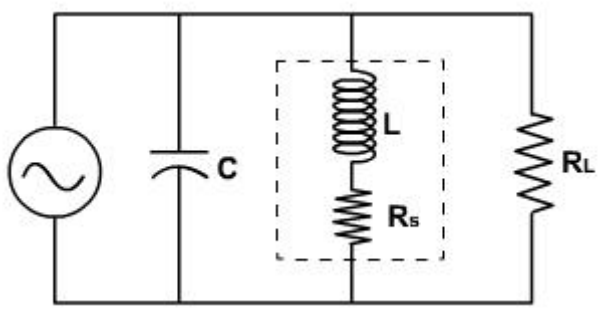

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Therefore,

$R_C = R_P \parallel R_L$

Q of the overall circuit = r_C / X_L

Current Sources

There are different methods of simulating a dc current source for integrated circuit amplifier biasing. One type of current source used to provide a fixed current is the fixed bias transistor circuit. The problem with this type of current source is that it requires too many resistors to be practically implemented on IC. The resistors in the following circuits are small and easy to fabricate on IC chips. When the current source is used to replace a large resistor the Thevenin resistance of the current source is the equivalent resistance value.

A simple current source

The simple two transistor current source shown in **fig. 1** is commonly used in ICs.

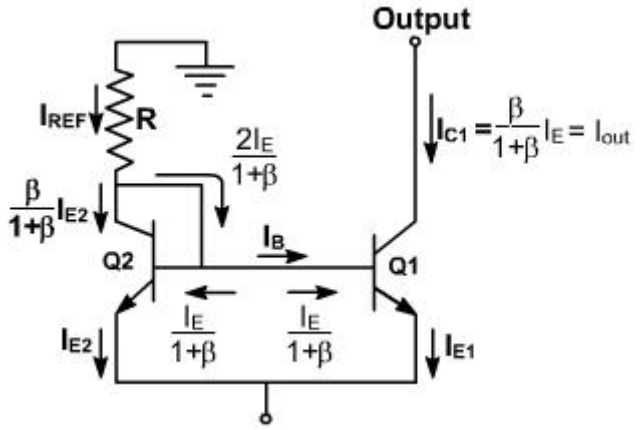


Fig. 1

A reference current is the input to a transistor connected as a diode. The voltage across this transistor drives the second transistor, where $R_E = 0$. Since the circuit has only one resistor, it can be easily fabricated on an IC chip.

The disadvantage of this circuit is that the reference current is approximately equal to the current source. In this circuit, Q_2 is in linear mode, since the collector voltage (output) is higher than the base voltage. The transistor Q_1 and Q_2 are identical devices fabricated on the same IC chip. The emitter currents are equal since the transistors are matched and emitters and bases are in parallel. If we sum the currents of Q_2, we obtain.

$I_B + I_C = I_E$

So $$I_{out} = I_{C1} = I_{E1}\frac{\beta}{1+\beta} = I_{E2}\frac{\beta}{1+\beta}$$

Summing currents at the collector of Q_1 we obtain

$$I_{REF} = \left(\frac{\beta}{1+\beta} + \frac{2}{1+\beta}\right) I_E = \frac{\beta+2}{1+\beta} I_E = I_O$$

If β is large, the current gain is approximately unity and the current mirror has reproduced the input current. One disadvantage of this current source is that its Thevenin resistance (R_{TH}) is limited by the r o ($1 / h_{oe}$) of the transistor. That is

$$R_{TH} = r_o = \frac{V_A}{I_C} \approx \frac{V_A}{I_{REF}}$$

Widlar Current Source

Large resistors are often required to maintain small currents of the order of few μA and these large resistors occupy correspondingly large areas on the IC chip. It is therefore, desirable to replace these large resistors with current sources. One such device is the Widlar current source as shown in **fig. 2**.

The two transistors are assumed perfectly matched. For the base circuit,

$$V_{BE1} - V_{BE2} - I_{E2}R_2 = 0 \qquad \text{(E-4)}$$

For a forward biased base-emitter junction diode, the emitter current is given by

$$i_E = I_0 e^{V_{BE}/nV_T}$$

Since $i_E \approx i_C = I_C$ and n = 1

$$I_C = I_0 e^{V_{BE}/V_T}$$

and $$V_{BE} = V_T \ln\left(\frac{I_C}{I_0}\right) \qquad \text{(E-5)}$$

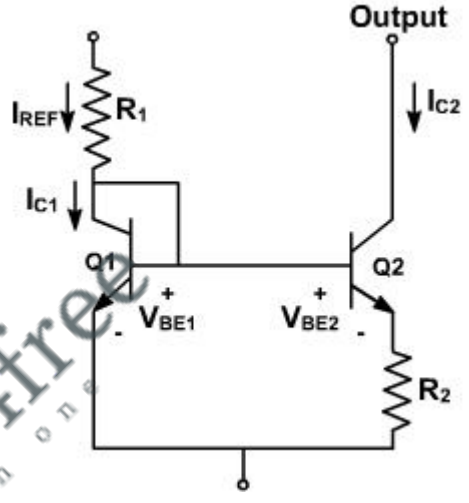


Fig. 2

Substituting V_{BE1} and V_{BE2} from (E-5) to (E-4), we get

$$V_T \ln\left(\frac{I_{C1}}{I_0}\right) - V_T \ln\left(\frac{I_{C2}}{I_0}\right) - I_{E2}R_2 = 0 \qquad \text{(E-6)}$$

We have assumed that both the transistors are matched so that I_{CO}, β and V_T are the same for both the transistors. Thus

$$V_T \ln\left(\frac{I_{C2}}{I_{C1}}\right) = I_{E2}R_2 \approx I_{C2}R_2$$

Hence, $$R_2 = \frac{V_T}{I_{C2}} \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$ (E-7)

where, $$I_{C1} = \frac{V_{CC} - V_{BE}}{R_1}$$ (E-8)

For design purposes, I_{C1} is usually known since it is used as the reference for all current sources on the entire chip and I_{C2} is t he desired output current. The Widlar circuit can also be used to simulate a high resistance.

Example-1

Design a Widlar current source to provide a constant current source of 3 ❖A with V_{CC} = 12V, R_1 = 50 kO, β =100 and V_{BE} = 0.7V

Solution:

The circuit is given in **fig.2** . Applying KVL to the Q_1 transistor we get,

$$I_{C1} = I_{REF} = \frac{12 - 0.7}{5 \times 10^3} = 0.226 \text{ mA}$$

Using the equation (E-7) we can calculate R_2

$$3 \times 10^{-6} R_2 = 0.025 \ln\left(\frac{2.26 \times 10^{-4}}{3 \times 10^{-6}}\right)$$

or $R_2 = 36\ k\Omega$

Wilson Current Source

Another current source transistor configuration that provides a very large parallel resistance is the Wilson current source which uses three transistors and provides this capability an the output is almost independent of the internal transistor characteristics. The Wilson current source as shown in **fig. 3**, uses the negative feedback provided by Q_3 to raise the output impedance

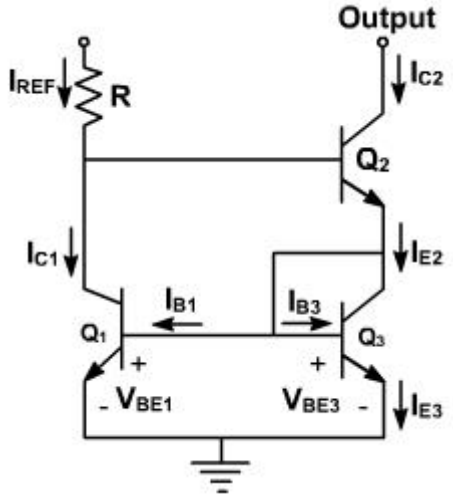


Fig. 3

The difference between the reference current and I_{C1} is the base current of Q_2.

$I_{E2} = (\beta + 1)\, I_{B2} = I_{C3}$ (E-9)

Since the base of Q_1 is connected to the base of Q_3, the currents in Q_1 are approximately independent of the voltage of the collector of Q_2. As such, the collector current of Q_2 remains almost constant providing high output impedance.

Let us now see that I_{C2} is approximately equal to I_{REF}. Applying Kirchhoff's current law at the emitter of Q_2 yields

$I_{E2} = I_{C3} + I_{B3} + I_{B1}$ (E-10)

Using the relationship between collector and base currents

$$I_{E2} = I_{C3}\left(1 + \frac{1}{\beta}\right) + \frac{I_{C1}}{\beta} \qquad \text{(E-11)}$$

Since all three transistors are matched, $V_{BE1} = V_{BE2} = V_{BE3}$ and $\beta_1 = \beta_2 = \beta_3$

With identical transistors, current in the feedback path splits equally between the bases of Q_1 and Q_3 leading so that $I_{B1} = I_{B3}$ and therefore $I_{C1} = I_{C3}$. Thus, the emitter current of Q_2 becomes

$$I_{E2} = I_{C3}\left(1 + \frac{2}{\beta}\right) \quad \text{(E-12)}$$

The collector current of Q_2 is

$$I_{C2} = \frac{I_{E2}\,\beta}{1+\beta} = \frac{I_{C3}\,(1 + 2/\beta)\,\beta}{1+\beta} \quad \text{(E-13)}$$

Solving for I_{C3} yields

$$I_{C3} = \frac{I_{C2}\,(1+\beta)}{\beta\,(1+2/\beta)} = I_{C2}\,\frac{1+\beta}{2+\beta} \quad \text{(E-14)}$$

Summing currents at the base of Q_2,

$$I_{C1} = I_{REF} - \frac{I_{C2}}{\beta} \quad \text{(E-15)}$$

$$I_{C2} = (I_{REF} - I_{C1}) \quad \text{(E-16)}$$

Since $I_{C1} = I_{C3}$, we substitute I_{C3} to obtain

$$I_{C2} = \beta I_{REF} - \frac{\beta\,(1+\beta)}{\beta+2}\,I_{C2} \quad \text{(E-17)}$$

and solving for I_{C2}

$$I_{C2} = \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2}\,I_{REF} = \left[1 - \frac{2}{\beta^2 + 2\beta + 2}\right] I_{REF} \quad \text{(E-18)}$$

Equation (E-10) shows that β has little effect upon I_{C2} since, for reasonable values of β.

$$\frac{2}{\beta^2 + 2\beta + 2} << 1 \quad \text{(E-19)}$$

Therefore, $I_{C2} = I_{REF}$

Multiple Current sources Using Current Mirrors

A number of current sources can be obtained from a single reference voltage. If the current is approximately the same as the reference voltage, the simple current source can be used as shown in **fig. 4** for Q_2 and Q_3.

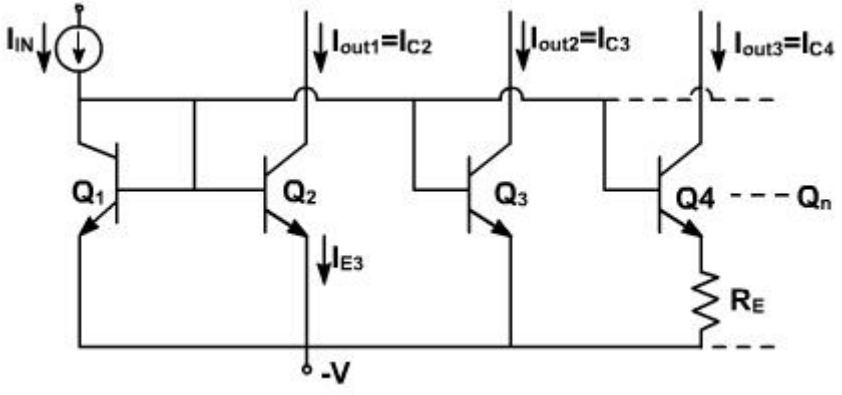


Fig. 4

Notice that Q_4 has an emitter resistance, which makes the current source a Widlar current source. Thus the amount of current delivered by this source can be determined by the size of the emitter resistor. This type of circuit is useful in integrated circuit chips as the one reference circuit can be used to develop current sources throughout the chip. When using the Widlar circuit, the currents can be different from the reference current.

The errors in base current, however, do accumulate when multiple outputs are used and the current gain tends to deviate from unity. In these types of circuits, lateral transistors can be used since it is not important that b be large. Lateral transistors usually have a β of approximately 20 which is more than adequate for current sources.

Example -2:

For the circuit shown in **fig. 5**, determine the emitter current in transistor Q_3. Given that β = 100, V_{BE} = 0.715V.

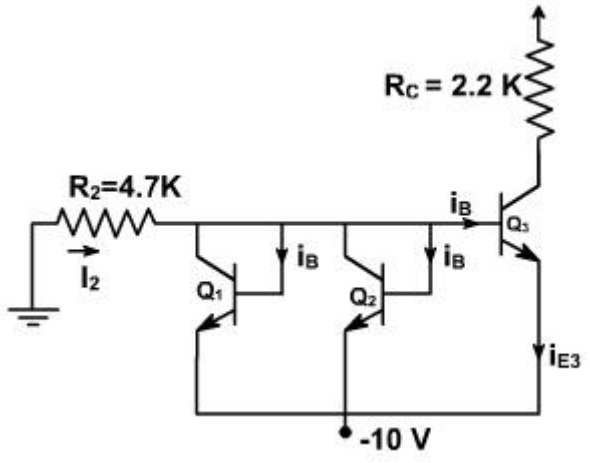


Fig. 5

Solution:

Since all transistor are identical, there V_{BE} voltage drop will be same.

$$\therefore I_2 = \frac{10 - 0.715}{4.7K}$$
$$= 1.976\ mA$$

Let I_B be the base current of each transistor and I_C be the collector current of Q_1 and Q_2.

Therefore,

$$2I_C + 3I_B = I_2$$
$$2 \times I_B + 3I_B = 1.976\ mA$$
$$\therefore I_B = 9.73\ A$$
$$I_E = (1+\beta)\, I_B$$
$$= 0.983\ mA$$

Example - 1

Determine the current and voltage gains for the two-stage capacitor-coupled amplifier shown in **fig. 1**.

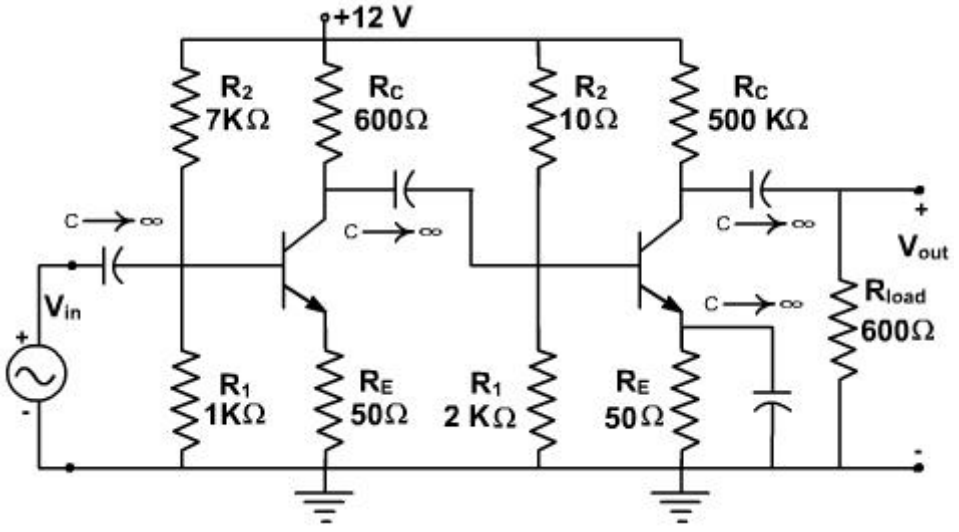


Fig. 1

Solution:

We develop the hybrid equivalent circuit for the multistage amplifier. This equivalent is shown in **fig. 2**. Primed variables denote output stage quantities and unprimed variables denote input stage quantities.

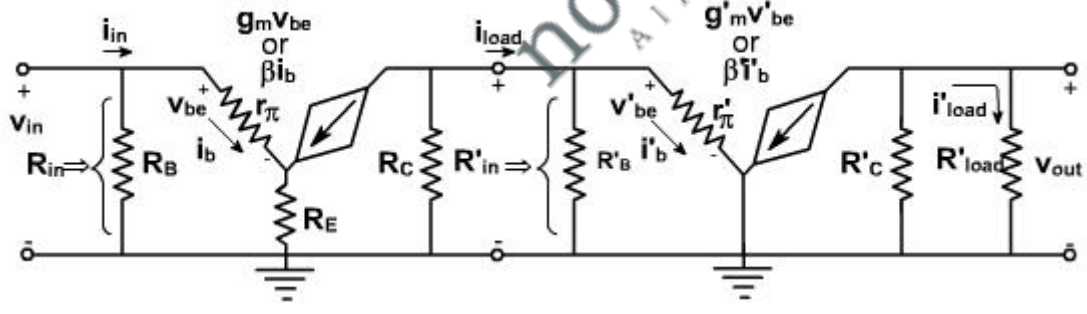


Fig. 2

Calculations for the output stages are as follows

$$R'_B = 10\,K\Omega \parallel 2\,K\Omega = \frac{10^4 \times 2 \times 10^3}{10^4 + 2 \times 10^3} = 1.67\,K\Omega$$

$$V'_{BB} = 12V \times \frac{2\,K\Omega}{10\,K\Omega + 2\,K\Omega} = \frac{12 \times 2 \times 10^3}{10^4 + 2 \times 10^3} = 2\,V$$

$$I'_{CQ} = \frac{V'_{BB} - V_{BE}}{R'_B/\beta + R'_B} = 22\,mA$$

$$r'_e = \frac{26(mV)}{I_{CQ}} = 1.77\ \ \Omega$$

For the input stage,

$$R_B = 7\,K\Omega \| 1K\Omega = \frac{7000 \times 1000}{7000 + 1000} = 875\ \Omega$$

$$V_{BB} = 12\,\frac{1K\Omega}{1\,K\Omega + 7\,K\Omega} = \frac{12 \times 1000}{700 + 1000} = 1.5\,V$$

$$I_{CQ} = \frac{1.5 - 0.7}{875/200 + 50} = 14.7\ \ mA$$

$$r_e' = \frac{26\ (mV)}{14.7\ (mA)} = 1.77\,\Omega$$

The input resistance is determined as:

$$R_{in} = R_B \| (r_\pi + \beta R_E) = \frac{875 \times 200 \times (1.77 + 50)}{875 + 10{,}354} = 807\ \Omega$$

The current gain, A_i, can be found by applying the equations derived earlier, where the first stage requires using the correct value for R_{load} derived form the value of R_{in} to the next stage.

Alternatively, we analyze **fig. 2** by extracting four current dividers as shown in **fig. 3**.

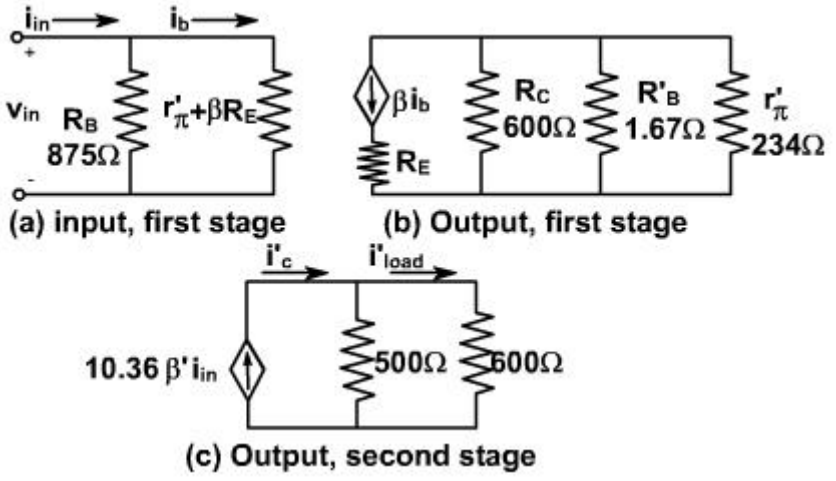


Fig. 3

The current division of the input stage is

$$i_b = \frac{R_B\, i_{in}}{R_B + r_\pi + \beta R_E} = 0.078\ i_{in}$$

The output of the first stage is coupled to the input of he second stage in **fig. 3(b)**. The input resistance of the second stage is

$$R'_{in} = R'_B \parallel r'_\pi = 205\ \Omega$$

The current in R'_{in} is i_{load} and is given by

$$i_{load} = \frac{15.6\, i_{in} \times 600}{805} = 11.6\, i_{in}$$

Again, i_{load} is current-divided at the input to the second stage. Thus,

$$i'_b = \frac{-R'_B\, i_{load}}{R'_B + r'_\pi} = -10.2\, i_{in}$$

The output current is found from **fig. 3(c)**:

$$i'_{load} = \frac{10.2\, i_{in} \times 200 \times 500}{500 + 600} = 927\ .\ i_{in}$$

The current gain is then

A_i =927

Now using the gain impedance formula, we find the voltage gain:

$$A_v = \frac{927 \times 600}{807} = 689$$

Impedance Coupling:

At higher frequency impedance coupling is used. The collector resistance is replaced by an inductor as shown in **fig. 4**. As the frequency increases, X_L approaches infinity and each inductor appears open. In other words, inductors pass dc but block ac. When used in this way, the inductors are called RFchokes.

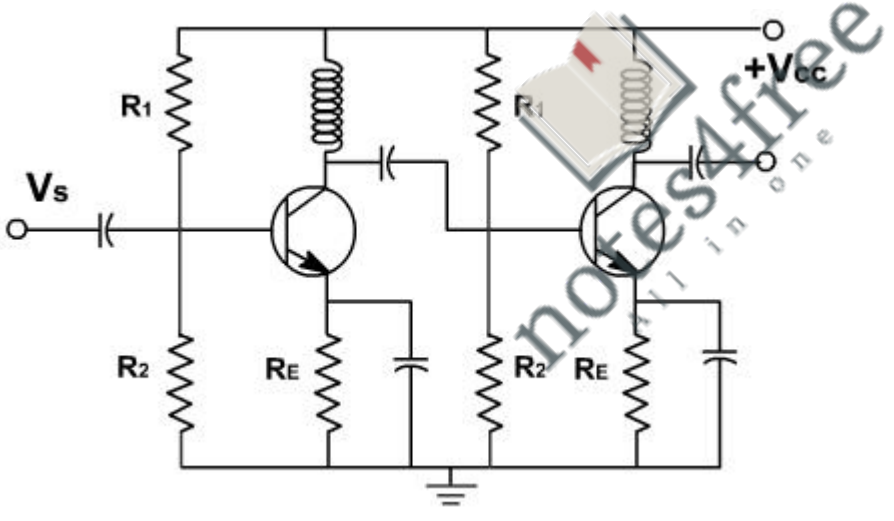


Fig. 4

The advantage is that no signal power is wasted in collector resistors. These RF chokes are relatively expensive and their impedance drops off at lower frequencies. It is suitable at radio frequency above 20 KHz.

Transformer Coupling:

In this case a transformer is used to transfer the ac output voltage of the first stage to the input of the second stage. **Fig. 5**, the resistors R_C is replaced by the primary winding of the

transformer. The secondary winding is used to give input to next stage. There is no coupling capacitor. The dc isolation between the two stages provided by the transformer itself. There is no power loss in primary winding because of low resistance.

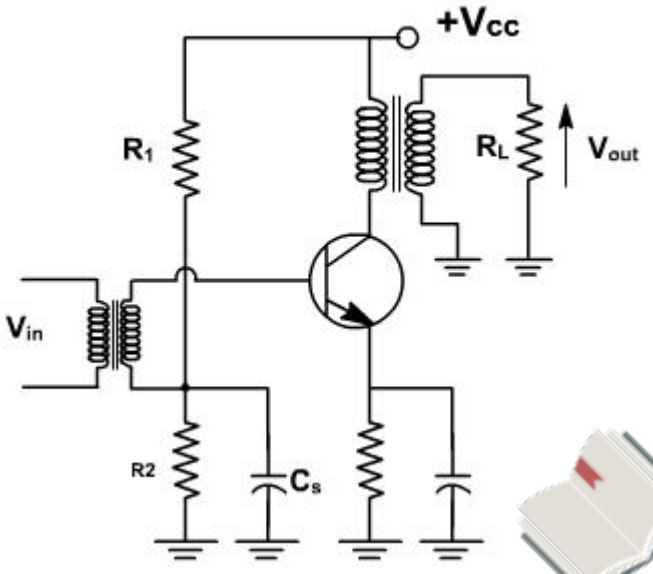


Fig. 5

At low frequency the size and cost of the transformer increases. Transformer coupling is still used in RF amplifiers. In AM radio receivers, RF signal have frequencies 550 to 1600 KHz. In TV receivers, the frequencies are 54 to 216 MHz. At these frequency the size and cost of the transformer reduces. C_S capacitor is used to make other point of transformer grounded, so that ac signal is applied between base and ground.

Tuned Transformer Coupling:

In this case a capacitor is shunted across primary winding to get resonance as shown in **fig. 6**. At this frequency the gain is maximum and at other frequencies the gain reduces very much. This allows us to filter out all frequencies except the resonant frequency and those near it. This is the principle behind tuning in a radio station or TV channel.

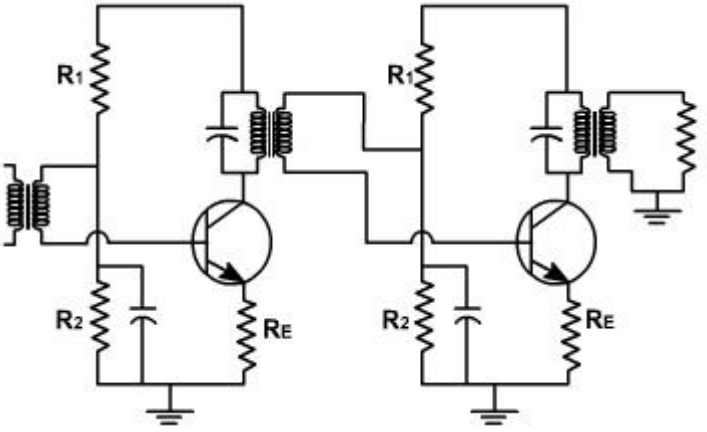


Fig. 6

Example - 2

Design a transformer-coupled amplifier as shown in **fig. 7** for a current gain of $A_i = 80$. Find the power supplied to the load and the power required from the supply.

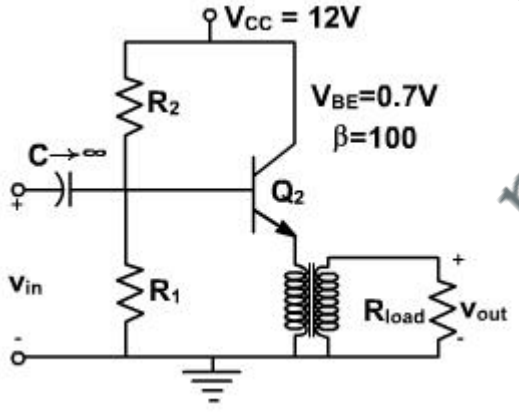


Fig. 7

Solution:

We first use the design equation to find the location of the Q-point for maximum output swing.

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}} = \frac{12}{a^2 R_{load}} = 23.4\text{mA}$$

Since the problem statement requires a current gain of 80, the amplifier must have a current gain of 10 because the transformer provides an additional gain of 8. We use the equations from Chapter 5 to find the base resistance R_B,

$$A_i = \frac{R_B}{R_B/\beta + r_e + R_E} = 10$$

where

$$R_E = a^2 R_{load} = 512\ \Omega$$

We note that r_e is sufficiently small to be neglected. Then, solving for R_B yields

$$R_B = 54.69\ K\Omega$$

$$V_{BB} = \frac{I_{CQ}R_B}{\beta} + V_{BE} = 2.03\ V$$

Now solving for the bias resistors,

$$R_1 = \frac{R_B}{1 + V_{BB}/V_{CC}} = 6.85\ K\Omega$$

$$R_2 = \frac{V_{CC}R_B}{V_{BB}} = 33.6\ K\Omega$$

The design is now complete. The power delivered by the source is given by

$$P_{V_{cc}} = V_{CC}I_{CQ} + \frac{V_{CC}^2}{R_1 + R_2} = 284\ mW$$

The power dissipated in the load is

$$P_{load} = \frac{(0.9a\, I_{CQ})^2 R_{load}}{2} = 114\ \ mW$$

We have restricted operation to the linear region by eliminating 5% of the maximum swing near cutoff and saturation. The efficiency is the ratio of the load to source power.

$$\eta = \frac{114}{284} = 0.4 \text{ or } 40\ \%$$

Oscillators

Objectives:

– To understand

• The basic operation of an Oscillator • the working of low frequency oscillators

– RC phase shift oscillator – Wien bridge Oscillator

• the working of tuned oscillator – Colpitt's Oscillator, Hartley Oscillator – Crystal Oscillator

• the working of UJT Oscillator

Basic operation of an Oscillator

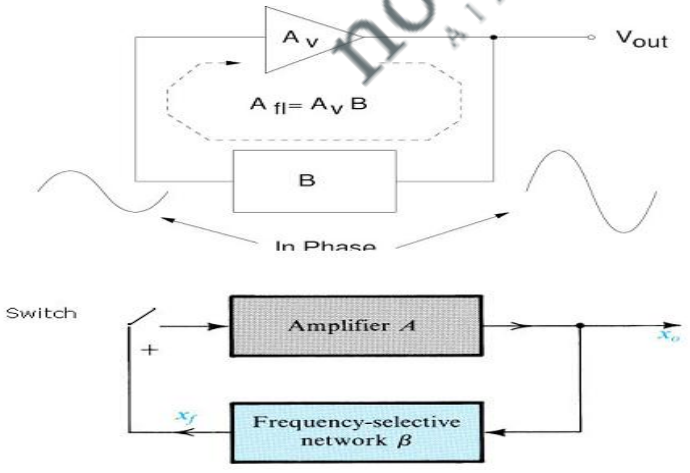
• An amplifier with positive feedback results in oscillations if the following conditions are satisfied:

– The loop gain (product of the gain of the amplifier and the gain of the feedback network) is unity

– The total phase shift in the loop is 0□

• If the output signal is sinusoidal, such a circuit is referred to as sinusoidal oscillator.

When the switch at the amplifier input is open, there are no oscillations. Imagine that a voltage Vi is fed to the circuit and the switch is closed. This results in V



When the switch at the amplifier input is open, there are no oscillations. Imagine that a voltage Vi is fed to the circuit and the switch is closed. This results in $V_o = A_V V_i$ and $\beta V_o = V_f$ is fed back to the circuit. If we make Vf = V then even if we remove the input voltage to the circuit, the output continues to exist.

$V_o = A_V V_i$

$\beta V_o = V_f$

$\beta A_V V_i = V_f$

If V_f has to be same as V_i, then from the above equation, it is clear that, □ A =1V

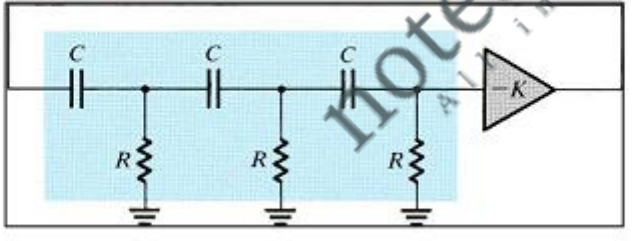
Thus in the above block diagram, by closing the switch and removing the input, we are able to get the oscillations at the output if □ AV =1, where □ A is called the **Loop gain**.

Positive feedback refers to the fact that the fed back signal is in phase with the input signal. This means that the signal experiences 0□ phase shift while traveling in the loop. The above condition along with the unity loop gain needs to be satisfied to get the sustained oscillations. These conditions are referred to as 'Barkhausen criterion'. Another way of seeing how the feedback circuit provides operation as an oscillator is obtained by noting the denominator in the basic equation

Af = A / (1+□ A).

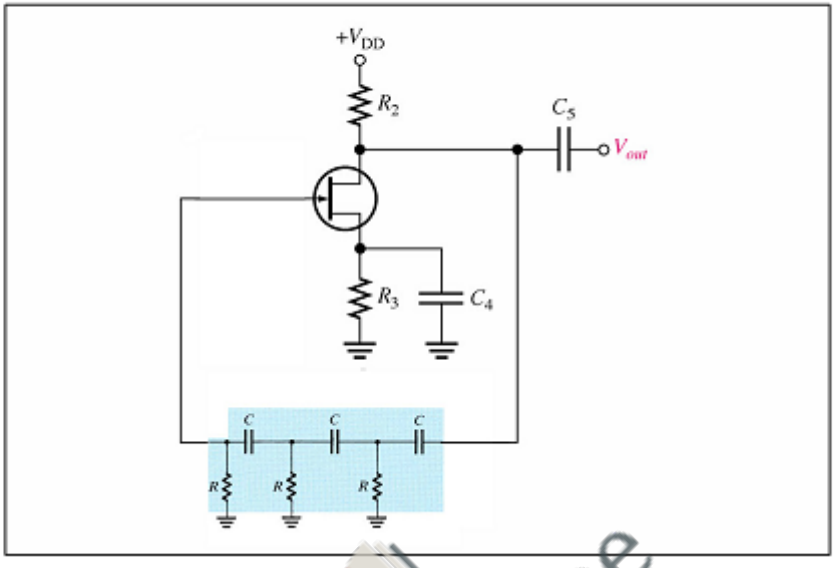
When □ A =-1 or magnitude 1 at a phase angle of 180□ , the denominator becomes 0 and the gain with feedback Af becomes infinite.Thus, an infinitesimal signal (noise voltage) can provide a measurable output voltage, and the circuit acts as an oscillator even without an input signal.

Phase shift oscillator



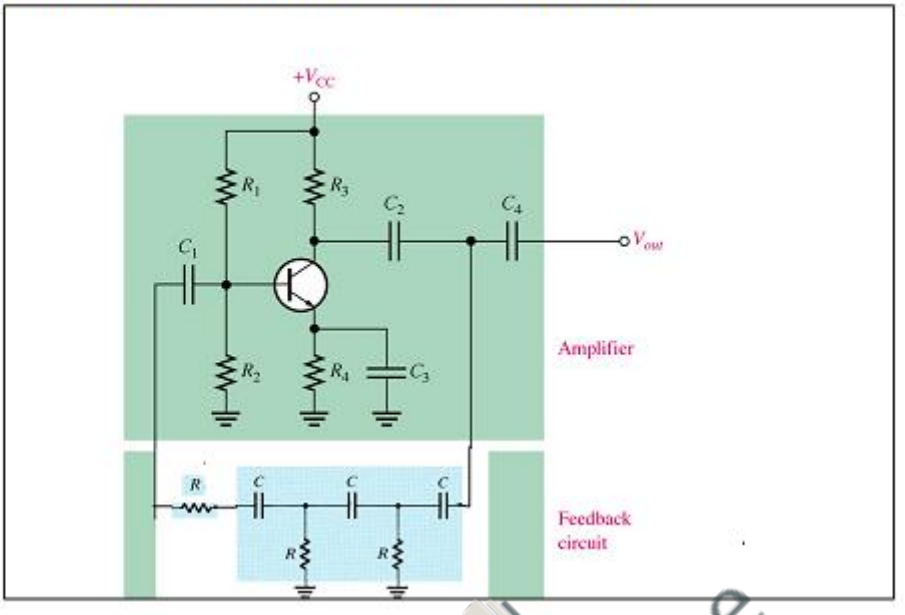
- The phase shift oscillator utilizes three RC circuits to provide 180º phase shift that when coupled with the 180º of the op-amp itself provides the necessary feedback to sustain oscillations.
- The gain must be at least 29 to maintain the oscillations. The frequency of resonance for the this type is similar to any RC circuit oscillator: $f_r = 1/2\sqrt{6}\pi RC$

FET phase shift oscillator



- The amplifier stage is self biased with a capacitor bypassed source resistor Rs and a drain bias resistor Rd . The FET device parameters of interest are gm and rd.
- $|A| = g_m R_L$, where $R_L = (R_D r_d / R_D + r_d)$
- At the operating frequency, we can assume that the input impedance of the amplifier is infinite .
- This is a valid approximation provided, the oscillator operating frequency is low enough so that FET capacitive impedances can be neglected.
- The output impedance of the amplifier stage given by R should also be small compared to the impedance seen looking into the feedback network so that no attenuation due to loading occurs.

RC Phase shift Oscillator - BJT version



• If a transistor is used as the active element of the amplifier stage, the output of thfeedback network is loaded appreciably by the relatively low input resistance (h ie) of the transistor.

• An emitter – follower input stage followed by a common emitter amplifier stage could be used.If a single transistor stage is desired, the use of voltage – shunt feedback is more suitable. Here, the feedback signal is coupled through the feedback resistor R' in series with the amplifier stage input resistance (R i).

$f = (1/2\pi RC)[1/\sqrt{6 + 4(RC / R)}]$

$h_{fe} > 23 + 29\ (R/RC) + 4\ (RC / R)$

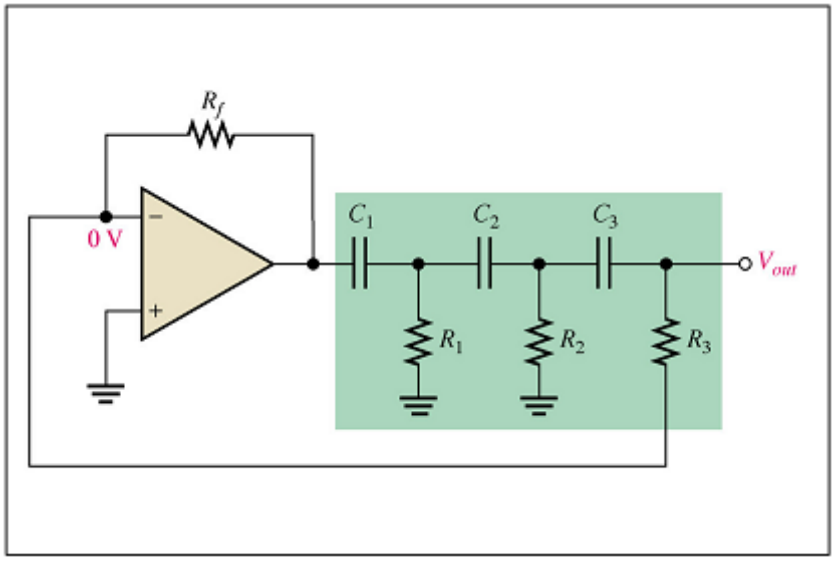
Problem:

It is desired to design a phase shift oscillator using an FET having g = 5000 □ S rd= 40 k□ , and a feedback circuit value of R = 10 k□ . Select the value of C for oscillator operation at 5 kHz and RD for A > 29 to ensure oscillator action.

Solution:

- $f = 1/2\sqrt{6}RC$; $C = 1/2\sqrt{6}Rf = 1.3nF$
- $|A| = g_m R_L$

  $Let\ A = 40;\ RL = |A| / gm = 8\ k\Omega$



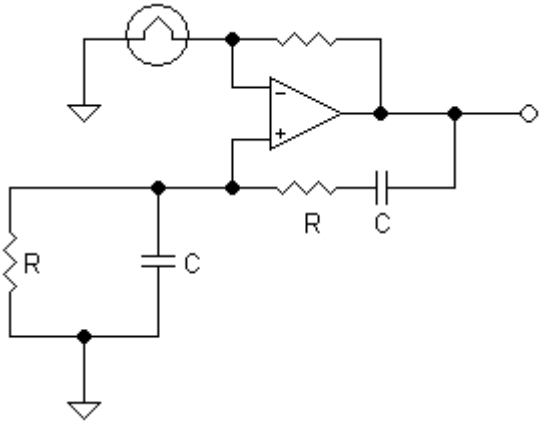
Wien bridge oscillator

A **Wien bridge oscillator** is a type of electronic oscillator that generates sine waves. It can generate a large range of frequencies. The circuit is based on an electrical network originally developed by Max Wien in 1891. The bridge comprises four resistors and two capacitors. It can also be viewed as a positive feedback system combined with a bandpass filter. Wien did not have a means of developing electronic gain so a workable oscillator could not be realized.

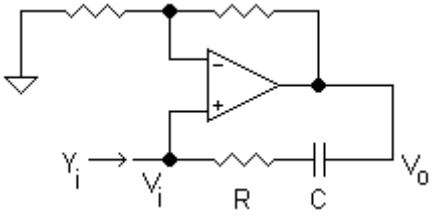
The modern circuit is derived from William Hewlett's 1939 Stanford University master's degree thesis. Hewlett, along with David Packard co-founded Hewlett-Packard. Their first product was the HP 200A, a precision sine wave oscillator based on the Wien bridge. The 200A was one of the first instruments to produce such low distortion.

The frequency of oscillation is given by:

$$f = \frac{1}{2\pi RC}$$



Analysis



Input admittance analysis

If a voltage source is applied directly to the input of an **ideal** amplifier with feedback, the input current will be:

$$i_{in} = \frac{v_{in} - v_{out}}{Z_f}$$

Where v_{in} is the input voltage, v_{out} is the output voltage, and Z_f is the feedback impedance. If the voltage gain of the amplifier is defined as:

$$A_v = \frac{v_{out}}{v_{in}}$$

And the input admittance is defined as:

$$Y_i = \frac{i_{in}}{v_{in}}$$

Input admittance can be rewritten as:

$$Y_i = \frac{1 - A_v}{Z_f}$$

For the Wien bridge, Z_f is given by:

$$Z_f = R + \frac{1}{j\omega C}$$

$$Y_i = \frac{(1 - A_v)\left(\omega^2 C^2 R + j\omega C\right)}{1 + (\omega C R)^2}$$

If A_v is greater than 1, the input admittance is a negative resistance in parallel with an inductance. The inductance is:

$$L_{in} = \frac{\omega^2 C^2 R^2 + 1}{\omega^2 C\left(A_v - 1\right)}$$

If a capacitor with the same value of C is placed in parallel with the input, the circuit has a natural resonance at:

$$\omega = \frac{1}{\sqrt{L_{in} C}}$$

Substituting and solving for inductance yields:

$$L_{in} = \frac{R^2 C}{A_v - 2}$$

If A_v is chosen to be 3:

$L_{in} = R^2 C$

Substituting this value yields:

$$\omega = \frac{1}{RC}$$

Or:

$$f = \frac{1}{2\pi RC}$$

Similarly, the input resistance at the frequency above is:

$$R_{in} = \frac{-2R}{A_v - 1}$$

For $A_v = 3$:

$R_{in} = -R$

If a resistor is placed in parallel with the amplifier input, it will cancel some of the negative resistance. If the net resistance is negative, amplitude will grow until clipping occurs. Similarly, if the net resistance is positive, oscillation amplitude will decay. If a resistance is added in parallel with exactly the value of *R*, the net resistance will be infinite and the circuit can sustain stable oscillation at any amplitude allowed by the amplifier.

Notice that increasing the gain makes the net resistance more negative, which increases amplitude. If gain is reduced to exactly 3 when a suitable amplitude is reached, stable, low distortion oscillations will result. Amplitude stabilization circuits typically increase gain until a suitable output amplitude is reached. As long as *R*, *C*, and the amplifier are linear, distortion will be minimal.

Crystal oscillator

A **crystal oscillator** is an electronic circuit that uses the mechanical resonance of a vibrating crystal of piezoelectric material to create an electrical signal with a very precise frequency. This frequency is commonly used to keep track of time (as in quartz wristwatches), to provide a stable clock signal for digital integrated circuits, and to stabilize frequencies for radio transmitters and receivers. The most common type of piezoelectric resonator used is the quartz crystal, so oscillator circuits designed around them were called "crystal oscillators".

Quartz crystals are manufactured for frequencies from a few tens of kilohertz to tens of megahertz. More than two billion (2×10^9) crystals are manufactured annually. Most are small devices for consumer devices such as wristwatches, clocks, radios, computers, and cellphones. Quartz crystals are also found inside test and measurement equipment, such as counters, signal generators, and oscilloscopes

A quartz crystal can be modeled as an electrical network with a low impedance (series) and a high impedance (parallel) resonance point spaced closely together. Mathematically (using the Laplace transform) the impedance of this network can be written as:

$$Z(s) = \left(\frac{1}{s \cdot C_1} + s \cdot L_1 + R_1\right) || \left(\frac{1}{s \cdot C_0}\right)$$

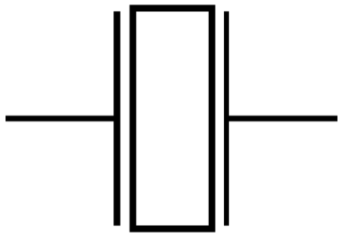
or,

$$Z(s) = \frac{s^2 + s\frac{R_1}{L_1} + {\omega_s}^2}{(s \cdot C_0)[s^2 + s\frac{R_1}{L_1} + {\omega_p}^2]}$$

$$\Rightarrow \omega_s = \frac{1}{\sqrt{L_1 \cdot C_1}}, \quad \omega_p = \sqrt{\frac{C_1 + C_0}{L_1 \cdot C_1 \cdot C_0}} = \omega_s\sqrt{1 + \frac{C_1}{C_0}} \approx \omega_s\left(1 + \frac{C_1}{2C_0}\right) \quad (C_0 \gg$$

where s is the complex frequency ($s = j\omega$), ω_s is the series resonant frequency in radians per second and ω_p is the parallel resonant frequency in radians per second.

Adding additional capacitance across a crystal will cause the parallel resonance to shift downward. This can be used to adjust the frequency at which a crystal oscillator oscillates. Crystal manufacturers normally cut and trim their crystals to have a specified resonance frequency with a known 'load' capacitance added to the crystal. For example, a 6 pF 32 kHz crystal has a parallel resonance frequency of 32,768 Hz when a 6.0 pF capacitor is placed across the crystal. Without this capacitance, the resonance frequency is higher than 32,768 Hz.



Module-5

Field Effect Transistor

The field effect transistor is a semiconductor device, which depends for its operation on the control of current by an electric field. There are two of field effect transistors:

1. JFET (Junction Field Effect Transistor)
2. MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

The FET has several advantages over conventional transistor.

1. In a conventional transistor, the operation depends upon the flow of majority and minority carriers. That is why it is called bipolar transistor. In FET the operation depends upon the flow of majority carriers only. It is called unipolar device.
2. The input to conventional transistor amplifier involves a forward biased PN junction with its inherently low dynamic impedance. The input to FET involves a reverse biased PN junction hence the high input impedance of the order of M-ohm.
3. It is less noisy than a bipolar transistor.
4. It exhibits no offset voltage at zero drain current.
5. It has thermal stability.
6. It is relatively immune to radiation.

The main disadvantage is its relatively small gain bandwidth product in comparison with conventional transistor.

Operation of FET:

Consider a sample bar of N-type semiconductor. This is called N-channel and it is electrically equivalent to a resistance as shown in **fig. 1**

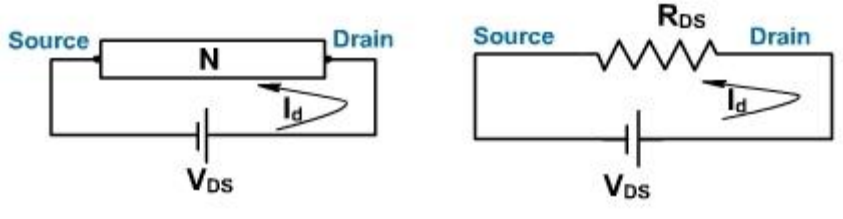


Fig. 1

Ohmic contacts are then added on each side of the channel to bring the external connection. Thus if a voltage is applied across the bar, the current flows through the channel.

The terminal from where the majority carriers (electrons) enter the channel is called source designated by S. The terminal through which majority carriers leaves the channel is called drain and designated by D. For an N-channel device, electrons are the majority carriers. Hence the circuit behaves like a dc voltage V_{DS} applied across a resistance R_{DS}. The resulting current is the drain current I_D. If V_{DS} increases, I_D increases proportionally.

Now on both sides of the n-type bar heavily doped regions of p-type impurity have been formed by any method for creating pn junction. These impurity regions are called gates (gate1 and gate2) as shown in **fig. 2**.

Both the gates are internally connected and they are grounded yielding zero gate source voltage (V_{GS} =0). The word gate is used because the potential applied between gate and source controls the channel width and hence the current.

As with all PN junctions, a depletion region is formed on the two sides of the reverse biased PN junction. The current carriers have diffused across the junction, leaving only uncovered positive ions on the n side and negative ions on the p side. The depletion region width increases with the magnitude of reverse bias. The conductivity of this channel is normally zero because of the unavailability of current carriers.

The potential at any point along the channel depends on the distance of that point from the drain, points close to the drain are at a higher positive potential, relative to ground, then points close to the source. Both depletion regions are therefore subject to greater reverse voltage near the drain. Therefore the depletion region width increases as we move towards drain. The flow of electrons from source to drain is now restricted to the narrow channel between the no conducting depletion regions. The width of this channel determines the resistance between drain and source.

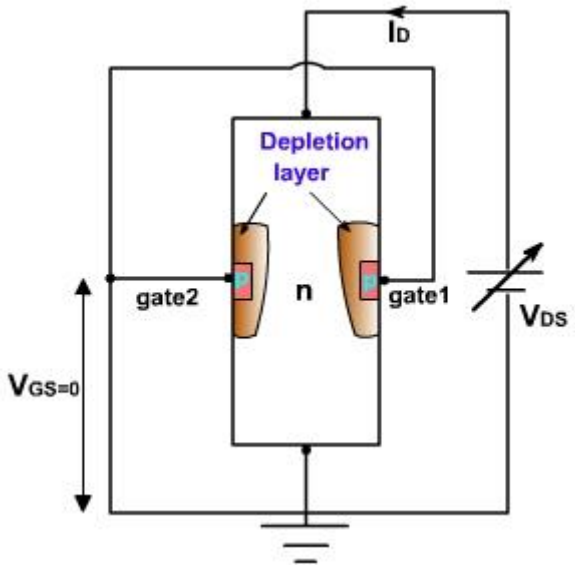


Fig. 2

Consider now the behavior of drain current I_D vs drain source voltage V_{DS}. The gate source voltage is zero therefore V_{GS}= 0. Suppose that V_{DS} is gradually linearly increased linearly from 0V. I_D also increases.

Since the channel behaves as a semiconductor resistance, therefore it follows ohm's law. The region is called ohmic region, with increasing current, the ohmic voltage drop between the source and the channel region reverse biased the junction, the conducting portion of the channel begins to constrict and I_D begins to level off until a specific value of V_{DS} is reached, called the **pinch of voltage V_P**.

At this point further increase in V_{DS} do not produce corresponding increase in I_D. Instead, as V_{DS} increases, both depletion regions extend further into the channel, resulting in a no more cross section, and hence a higher channel resistance. Thus even though, there is more voltage, the resistance is also greater and the current remains relatively constant. This is called pinch off or saturation region. The current in this region is maximum current that FET can produce and designated by I_{DSS}. (Drain to source current with gate shorted).

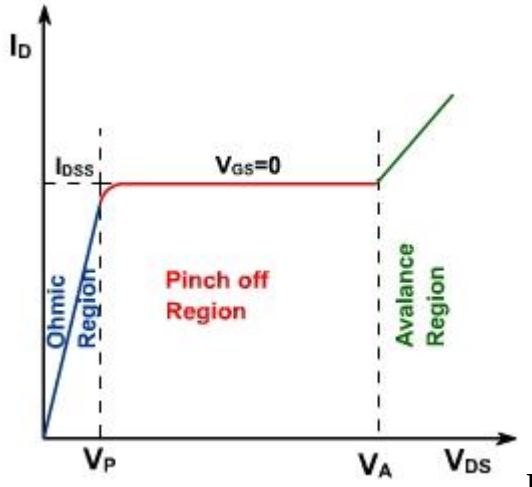


Fig. 3

As with all pn junctions, when the reverse voltage exceeds a certain level, avalanche breakdown of pn junction occurs and I_D rises very rapidly as shown in **fig. 3**.

Consider now an N-channel JFET with a reverse gate source voltage as shown in **fig. 4**.

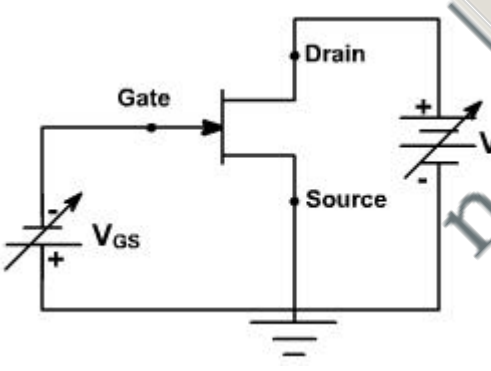


Fig. 4

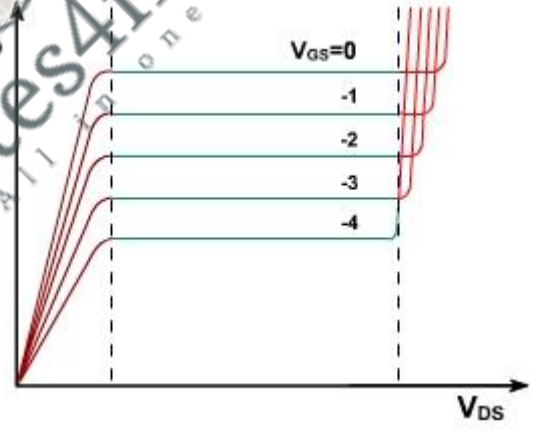


Fig. 5

The additional reverse bias, pinch off will occur for smaller values of $|V_{DS}|$, and the maximum drain current will be smaller. A family of curves for different values of V_{GS}(negative) is shown in **fig. 5**.

Suppose that V_{GS}= 0 and that due of V_{DS} at a specific point along the channel is +5V with respect to ground. Therefore reverse voltage across either p-n junction is now 5V. If V_{GS} is

decreased from 0 to ?1V the net reverse bias near the point is 5 - (-1) = 6V. Thus for any fixed value of V_{DS}, the channel width decreases as V_{GS} is made more negative.

Thus I_D value changes correspondingly. When the gate voltage is negative enough, the depletion layers touch each other and the conducting channel pinches off (disappears). In this case the drain current is cut off. The gate voltage that produces cut off is symbolized $V_{GS}(off)$. It is same as pinch off voltage.

Since the gate source junction is a reverse biased silicon diode, only a very small reverse current flows through it. Ideally gate current is zero. As a result, all the free electrons from the source go to the drain i.e. $I_D = I_S$. Because the gate draws almost negligible reverse current the input resistance is very high 10's or 100's of M ohm. Therefore where high input impedance is required, JFET is preferred over BJT. The disadvantage is less control over output current i.e. FET takes larger changes in input voltage to produce changes in output current. For this reason, JFET has less voltage gain than a bipolar amplifier.

Biasing the Field Effect Transistor

Transductance Curves:

The transductance curve of a JFET is a graph of output current (I_D) vs input voltage (V_{GS}) as shown in **fig. 1**.

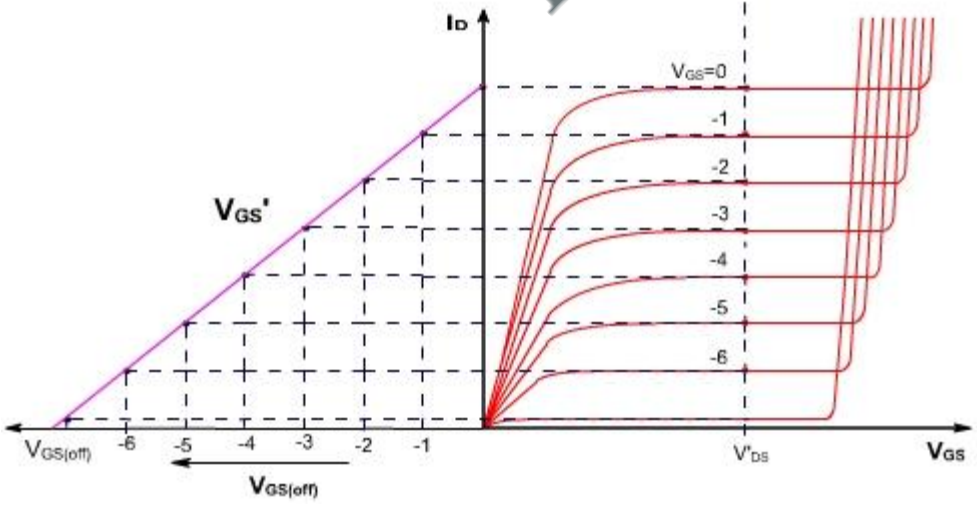


Fig. 1

By reading the value of I_D and V_{GS} for a particular value of V_{DS}, the transductance curve can be plotted. The transductance curve is a part of parabola. It has an equation of

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(Off)}}\right)^2$$

Data sheet provides only I_{DSS} and V_{GS}(off) value. Using these values the transductance curve can be plotted.

Biasing the FET:

The FET can be biased as an amplifier. Consider the common source drain characteristic of a JFET. For linear amplification, Q point must be selected somewhere in the saturation region. Q point is selected on the basis of ac performance i.e. gain, frequency response, noise, power, current and voltage ratings.

Gate Bias:

Fig. 2, shows a simple gate bias circuit.

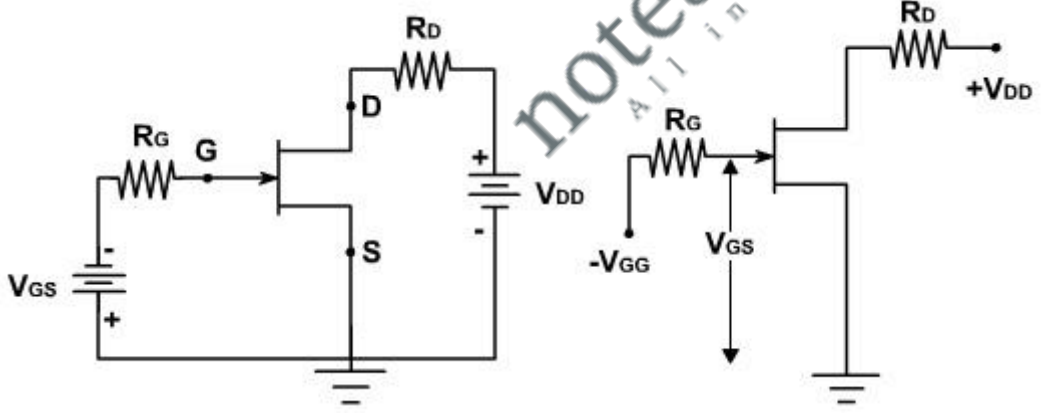


Fig. 2

Separate V_{GS} supply is used to set up Q point. This is the worst way to select Q point. The reason is that there is considerable variation between the maximum and minimum values of FET parameters e.g.

I_{DSS} V_{GS}(off)

Minimum	4mA	-2V
Maximum	13mA	-8V

This implies that the minimum and maximum transductance curves are displaced as shown in **fig. 3**.

Gate bias applies a fixed voltage to the gate. This fixed voltage results in a Q point that is highly sensitive to the particular JFET used. For instance, if V_{GS}= -1V the Q point may very from Q_1 to Q_2 depending upon the JFET parameter is use.

At Q_1, I_D= 0.016 (1 - (1/8))^2 = 12.3 mA

At Q_2, I_D= 0.004 (1-(1/2))^2 = 1 mA.

The variation in drain current is very large.

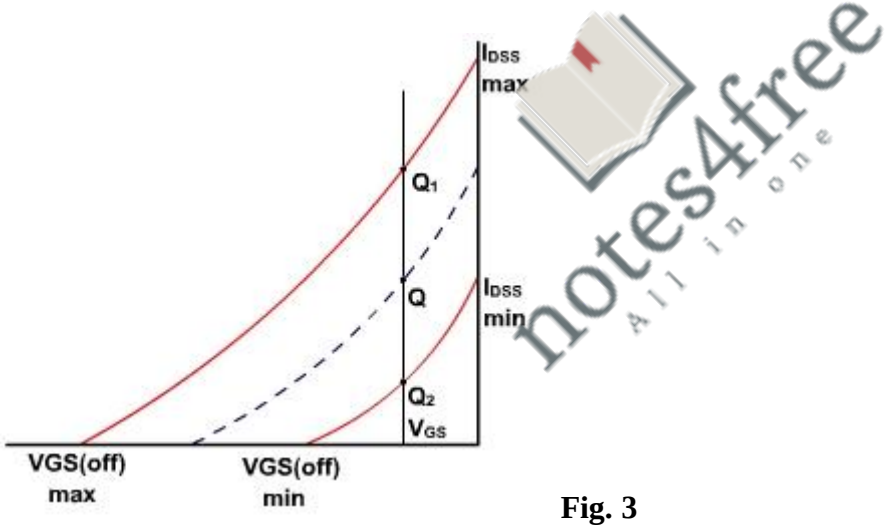


Fig. 3

Self Bias: **Fig. 4**, shows a self bias circuit another way to bias a FET. Only a drain supply is used and no gate supply. The idea is to use the voltage across R_S to produce the gate source reverse voltage.

This is a form of a local feedback similar to that used with bipolar transistors. If drain current increases, the voltage drop across R_S increases because the I_D R_S increases. This increases the gate source reverse voltage which makes the channel narrow and reduces the drain current. The overall effect is to partially offset the original increase in drain current. Similarly, if I_D decreases, drop across R_S decreases, hence reverse bias decreases and I_D increases.

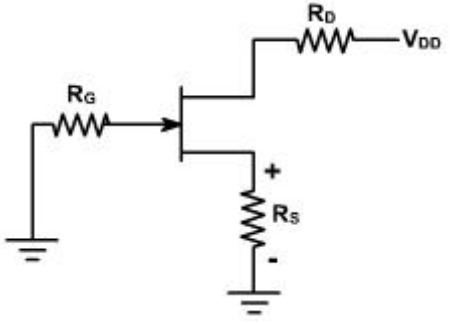


Fig. 4

Since the gate source junction is reverse biased, negligible gate current flows through R_G and so the gate voltage with respect to ground is zero.

$V_G = 0;$

The source to ground voltage equals the product of the drain current and the source resistance.

$\therefore V_S = I_D R_S.$

The gate source voltage is the difference between the gate voltage and the source voltage.

$V_{GS} = V_G - V_S = 0 - I_D R_S$

$V_{GS} = -I_D R_S.$

This means that the gate source voltage equals the negative of the voltage across the source resistor. The greater the drain current, the more negative the gate source voltage becomes.

Rearranging the equation:

$I_D = -V_{GS} / R_S$

The graph of this equation is called self base line a shown in **Fig. 5**.

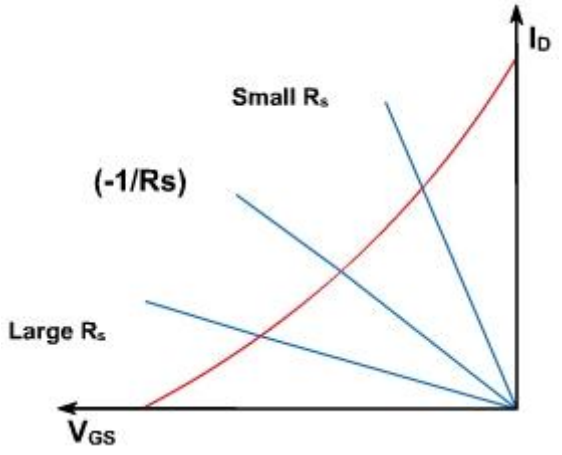


Fig. 5

The operating point on transductance curve is the intersection of self bias line and transductance curve. The slope of the line is ($-1 / R_S$). If the source resistance is very large ($-1 / R_S$ is small) then Q-point is far down the transductance curve and the drain current is small. When R_S is small, the Q point is far up the transductance curve and the drain current is large. In between there is an optimum value of R_S that sets up a Q point near the middle of the transductance curve.

The transductance curve varies widely for FET (because of variation in I_{DSS} and $V_{GS}(off)$) as shown in **fig. 6**. The actual curve may be in between there extremes. A and B are the optimum points for the two extreme curves. To find the optimum resistance R_S, so that Q-point is correct for all the curves, A and B points are joined such that it passes through origin.

The slope of this line gives the resistance value R_S($V_{GS} = -I_D R_S$). The current I_Q is such that $I_A > I_Q > I_B$. Here A, Q and B all points are in straight line.

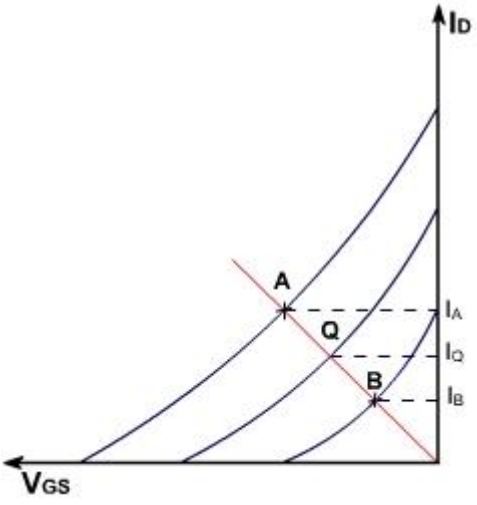


Fig. 6

Consider the case where a line drawn to pass between points A and B does not pass through the origin. The equation $V_{GS} = - I_D R_S$ is not valid. The equation of this line is $V_{GS} = V_{GG} ? I_D R_S$.

Such a bias relationship may be obtained by adding a fixed bias to the gate in addition to the source self bias as shown in **fig. 7**.

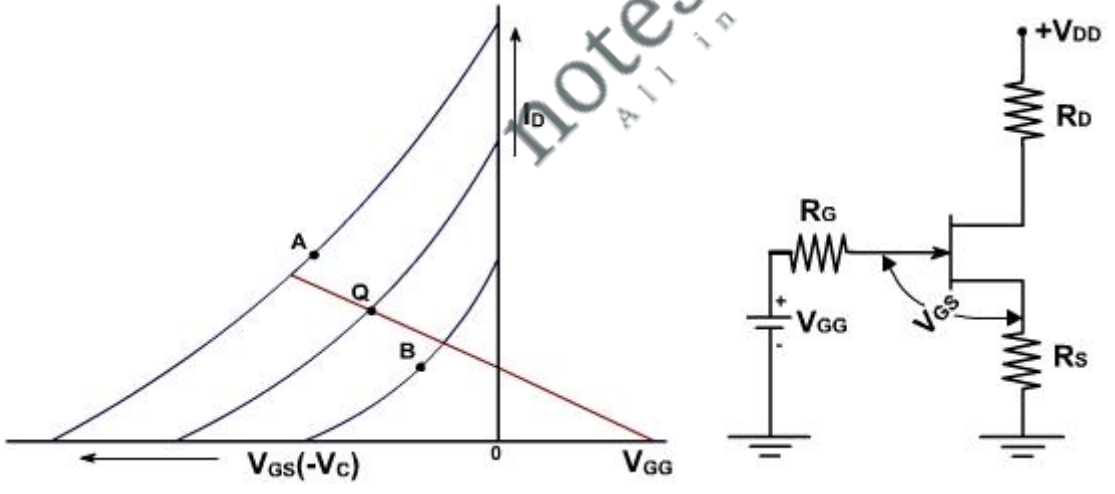


Fig. 7

In this circuit.

$V_{GG} = R_S I_G + V_{GS} + I_D R_S$

Since $R_S I_G = 0$;

$$V_{GG} = V_{GS} + I_D R_S$$

or $V_{GS} = V_{GG}? I_D R_S$

Voltage Divider Bias :

The biasing circuit based on single power supply is shown in **fig. 1**. This is similar to the voltage divider bias used with a bipolar transistor.

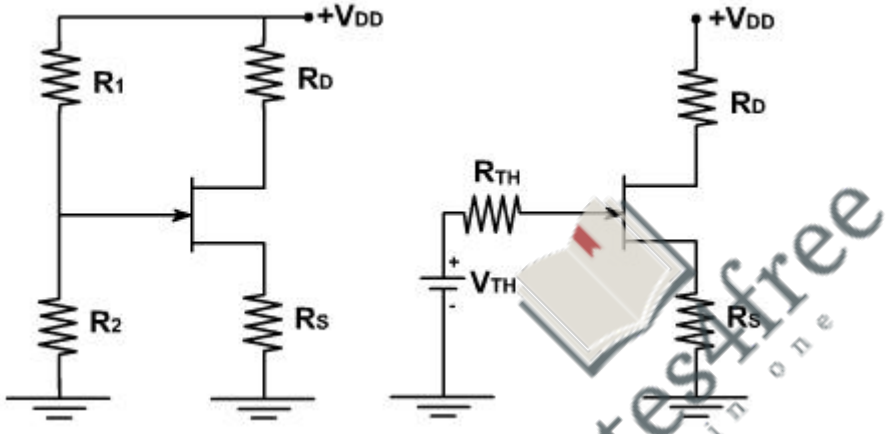


Fig. 1

The Thevenin voltage V_{TH} applied to the gate is

$$V_{TH} = \frac{R_2}{R_1 + R_2} V_{DD}$$

The Thevenin resistance is given as

$$R_{TH} = \frac{R_2 R_1}{R_1 + R_2}$$

The gate current is assumed to be negligible. V_{TH} is the dc voltage from gate to ground.

$$V_{TH} = V_{GS} + V_S \text{ (neglecting } I_G)$$
$$\therefore V_S = V_{TH} = V_{GS}$$

The drain current ID is given by

$$I_D = \frac{V_{TH} - V_{GS}}{R_S}$$

and the dc voltage from the drain to ground is $V_D = V_{DD} ? I_D R_D$.

If V_{TH} is large enough to swamp out V_{GS} the drain current is approximately constant for any JFET as shown in **fig. 2**.

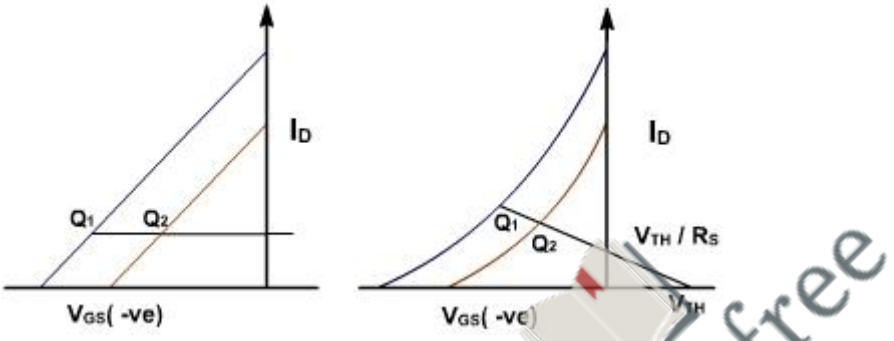


Fig. 2

There is a problem in JFET. In a BJT, V_{BE} is approximately 0.7V, with only minor variations from one transistor to other. In a FET, V_{GS} can vary several volts from one JFET to another. It is therefore, difficult to make V_{TH} large enough to swamp out V_{GS}. For this reason, voltage divider bias is less effective with, FET than BJT. Therefore, V_{GS} is not negligible. The current increases slightly from Q2 to Q1. However, voltage divider bias maintains I_D nearly constant.

Consider a voltage divider bias circuit shown in **fig. 3**.

$V_{GS(min)} = -1, \quad V_{GS(max)} = -5V$

$V_{TH} = 15V$

$I_{D(min)} = \frac{15-(-1)}{7.5K} = 2.13 \text{ mA}$

$I_{D(max)} = \frac{15-(-5)}{7.5K} = 2.67 \text{ mA}$

Difference in $I_{D\,(min)}$) and $I_{D\,(max)}$ is less

$V_{D\,(max)} = 30 ? 2.13 * 4.7 = 20 V$

$V_{D\,(min)} = 30 ? 2.67 * 4.7 = 17.5 V$

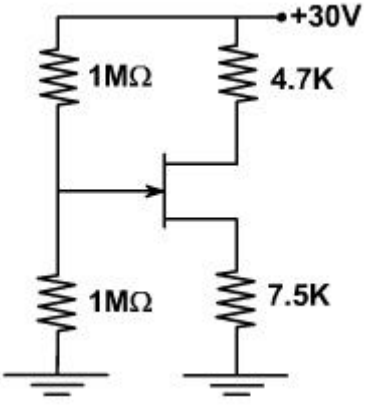


Fig. 3

Current Source Bias:

This is another way to produce solid Q point. The aim is to produce a drain current that is independent of V_{GS}. Voltage divider bias and self bias attempt to do this by swamping out of variations in V_{GS}.

Using two power supplies:

The current source bias can be used to make I_D constant **fig. 4**.

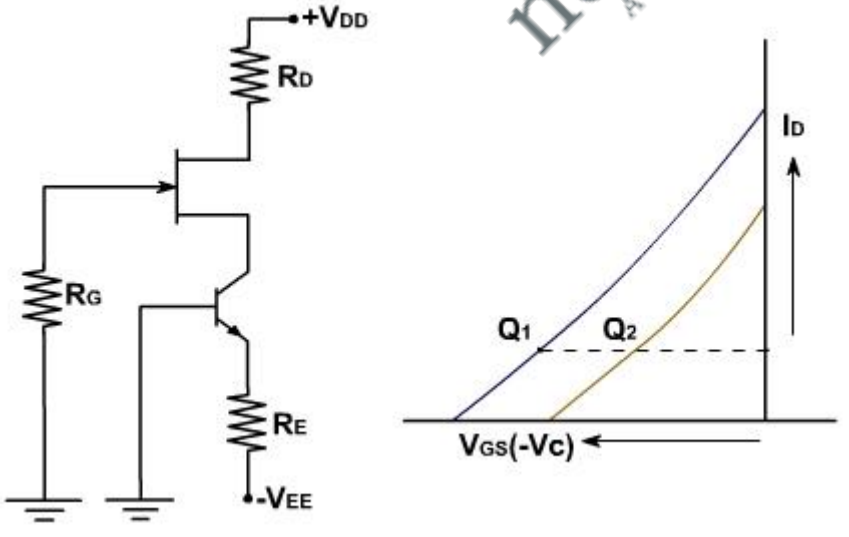


Fig. 4

The bipolar transistor is emitter biased; its collector current is given by

$I_C = (V_{EE} ? V_{BE}) / R_E$.

Because the bipolar transistor acts like a current source, it forces the drain current to equal the bipolar collector current.

$I_D = I_C$

Since I_C is constant, both Q points have the same value of drain current. The current source effectively wipes out the influence of V_{GS}. Although V_{GS} is different for each Q point, it no longer influences the value of drain current.

Using One power supply:

When only a positive supply is available, the circuit shown in **fig. 5**, can be used to set up a constant drain current.

In this case, the bipolar transistor is voltage divider biased. Assuming a stiff voltage divider, the emitter and collector currents are constant for all bipolar transistors. This forces the FET drain current equal the bipolar collector current.

$$V_{TH} = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$I_E = \frac{V_{TH} - V_{BE}}{R_E}$$

Since V_{TH} is constant, I_E is also constant

$$I_C = I_S = I_D = \text{constant}$$

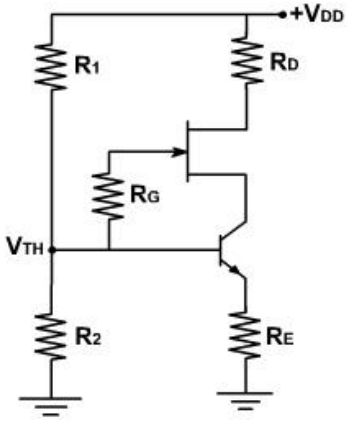


Fig. 5

Transductance: The transductance of a FET is defined as

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{gs}}\right|_{V_{DS}=0} \mu A/Volts$$

Because the changes in I_D and V_{GS} are equivalent to ac current and voltage. This equation can be written as

$$g_m = \left.\frac{i_d}{V_{gs}}\right|_{V_{ds}=0}$$

The unit of g_m is mho or siemems.

Typical value of g_m is 2000 m A / V.

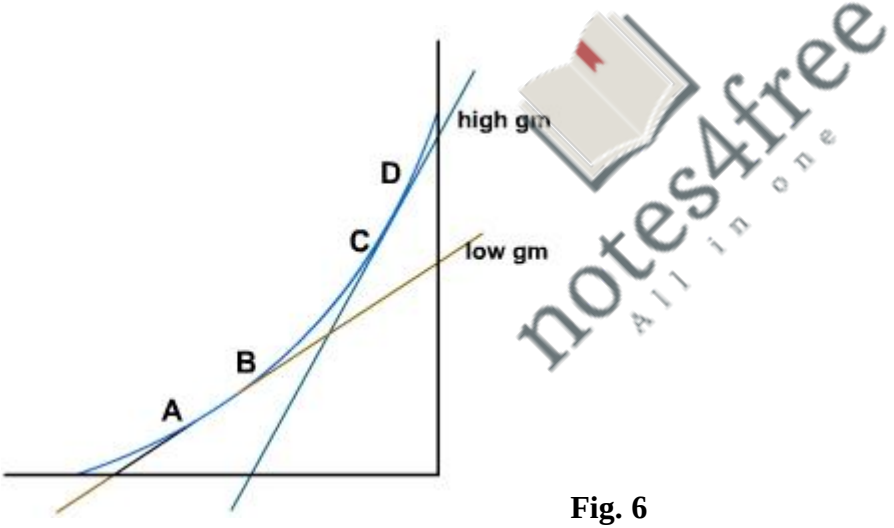


Fig. 6

The value of g_m can be obtained from the transductance curve as shown in **fig. 6**.

If A and B points are considered, than a change in V_{GS} produces a change in I_D. The ratio of I_D and V_{GS} is the value of g_m between A and B points. If C and D points are considered, then same change in V_{GS} produces more change in I_D. Therefore, g_m value is higher. In a nutshell, g_m tells us how much control gate voltage has over drain current. Higher the value of g_m, the more effective is gate voltage in controlling gate current. The second parameter r_d is the drain resistance.

$$r_d = \frac{v_{ds}}{i_d}\Big|_{v_{gs}=0} \quad (r_d \text{ is negligible})$$

FET a amplifier

Similar to Bipolar junction transistor. JFET can also be used as an amplifier. The ac equivalent circuit of a JFET is shown in **fig. 1**.

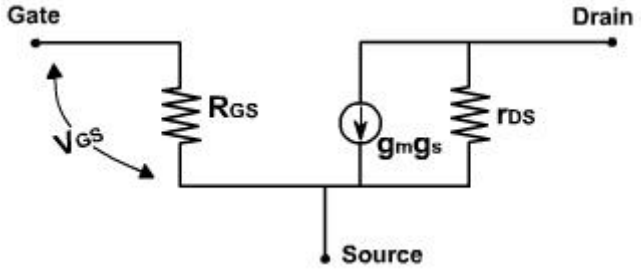


Fig. 1

The resistance between the gate and the source R_{GS} is very high. The drain of a JFET acts like a current source with a value of $g_m V_{gs}$. This model is applicable at low frequencies.

From the ac equivalent model

$$i_d = g_m V_{gs} + \frac{V_{ds}}{r_d}$$

$$\text{When } i_d = 0, \quad \frac{V_{ds}}{V_{gs}} = -g_m r_d$$

The amplification factor μ for FET is defined as

$$\mu = \frac{v_{ds}}{v_{gs}}\Big|_{i_d=0} \quad \therefore \mu = g_m r_d$$

When $V_{GS} = 0$, g_m has its maximum value. The maximum value is designated as g_{mo}. Again consider the equation,

$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = 2I_{DSS}\left[1-\frac{V_{GS}}{V_{GS(off)}}\right]\left[\frac{-1}{V_{GS(off)}}\right]$$

$$g_m = \frac{-2I_{DSS}}{V_{GS(Off)}}\left[1-\frac{V_{GS}}{V_{GS(off)}}\right]$$

When $V_{GS} = 0$, $g_m = g_{mo} = \frac{-2I_{DSS}}{V_{GS(off)}}$

$$\therefore g_m = g_{mo}\left[1-\frac{V_{GS}}{V_{GS(off)}}\right]$$

As V_{GS} increases, gm decreases linearly.

$$V_{GS(off)} = \frac{-2I_{DSS}}{g_{mo}}$$

Measuring I_{DSS} and g_m, $V_{GS(off)}$ can be determined

FET as Amplifier:

Fig. 2, shows a common source amplifier.

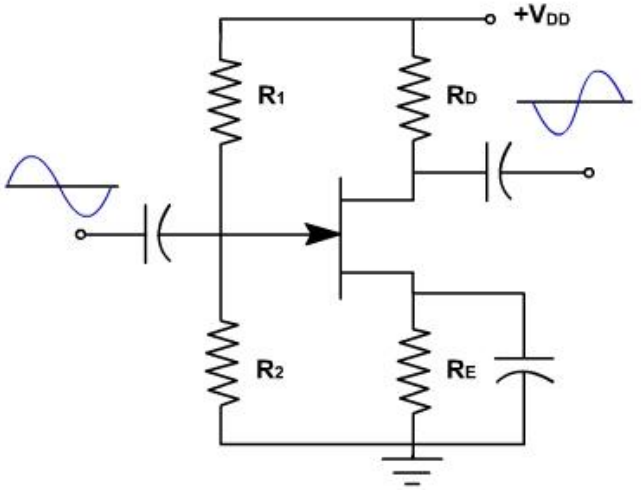


Fig. 2

When a small ac signal is coupled into the gate it produces variations in gate source voltage. This produces a sinusoidal drain current. Since an ac current flows through the drain resistor. An amplified ac voltage is obtained at the output. An increase in gate source voltage produces more drain current, which means that the drain voltage is decreasing. Since the positive half cycle of input voltage produces the negative half cycle of output voltage, we get phase inversion in a CS amplifier.

The ac equivalent circuit is shown in **fig. 3**.

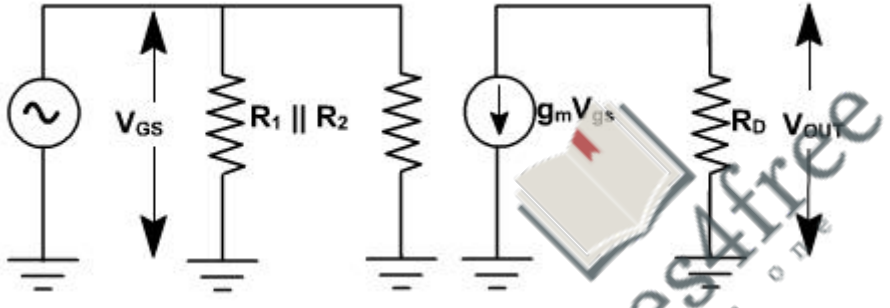


Fig. 3

The ac output voltage is

$v_{out} = - g_m v_{gS} R_D$

Negative sign means phase inversion. Because the ac source is directly connected between the gate source terminals therefore ac input voltage equals

$V_{in} = V_{gs}$

The voltage gain is given by

$$A_V = \frac{v_{out}}{v_{in}} = - g_m R_D$$

$A_V =$ unloaded voltage gain

The further simplified model of the amplifieris shown in **fig. 4**.

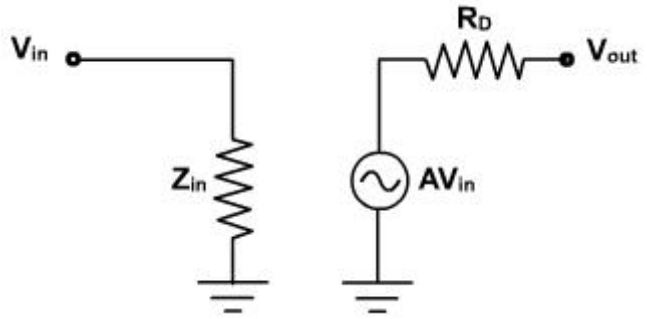


Fig. 4

Z_{in} is the input impedance. At low frequencies, this is parallel combination of $R_1 || R_2 || R_{GS}$. Since R_{GS} is very large, it is parallel combination of R_1 & R_2. A V_{in} is output voltage and R_D is the output impedance.

Because of nonlinear transductance curve, a JFET distorts large signals, as shown in **fig. 5**.

Given a sinusoidal input voltage, we get a non-sinusoidal output current in which positive half cycle is elongated and negative cycle is compressed. This type of distortion is called Square law distortion because the transductance curve is parabolic.

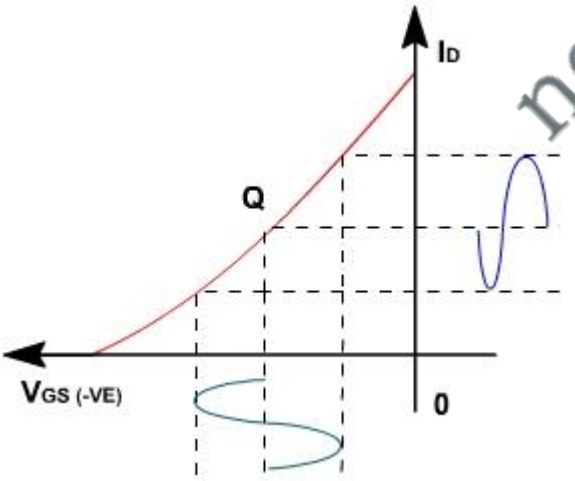


Fig. 5

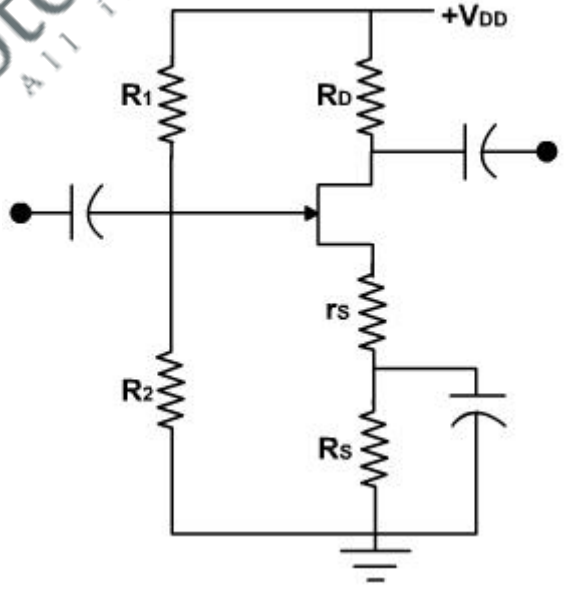


Fig. 6

This distortion is undesirable for an amplifier. One way to minimize this is to keep the signal small. In that case a part of the curve is used and operation is approximately linear. Some

times swamping resistor is used to minimize distortion and gain constant. Now the source is no longer ac ground as shown in **fig. 6**.

The drain current through r_S produces an ac voltage between the source and ground. If r_S is large enough the local feedback can swamp out the non-linearity of the curve. Then the voltage gain approaches an ideal value of R_D / r_S.

Since R_{GS} approaches infinity therefore, all the drain current flows through r_S producing a voltage drop of $g_m V_{gS} r_S$. The ac equivalent circuit is shown in **fig. 7**.

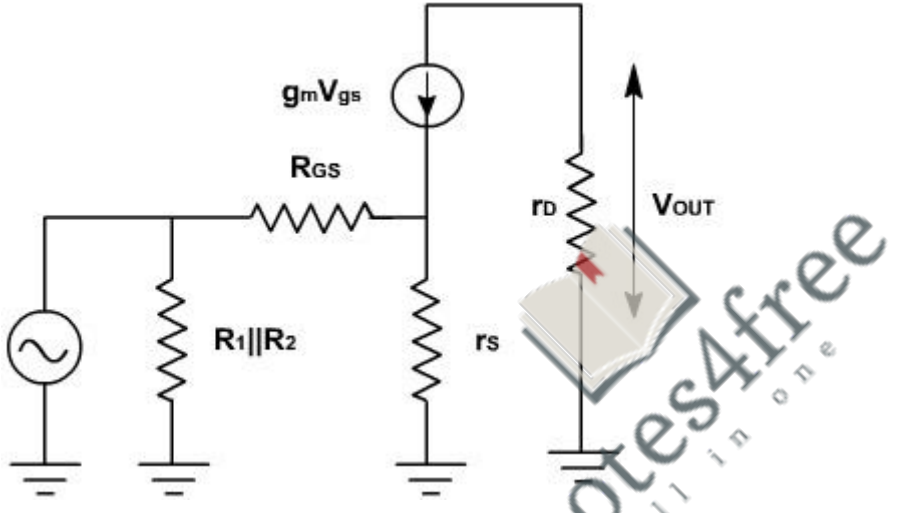


Fig. 7

$$v_{gs} + g_m \; v_{gs} \cdot r_s - v_{in} = 0$$

$$v_{in} = (1 + g_m r_s) \; v_{gs}$$

$$v_{out} = - g_m R_D \; v_{gs}$$

$$A = \frac{- g_m R_D}{1 + g_m r_s} = \frac{-R_D}{r_s + 1/g_m}$$

The voltage gain reduces but voltage gain is less effective by change in g_m. r_S must be greater than 1 / g_m only then

$$v_{gs} = - \frac{R_D}{r_s}$$

JFET Applications

Example-1:

Determine gm for an n-channel JFET with characteristic curve shown in **fig. 1**.

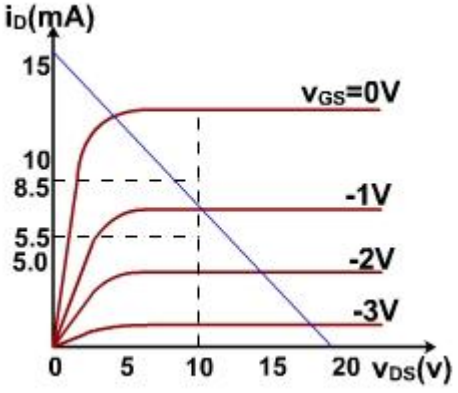


Fig. 1

Solution:

We select an operating region which is approximately in the middle of the curves; that is, between v_{GS} = -0.8 V and v_{GS} = -1.2 V; i_D = 8.5mA and i_D = 5.5 mA. Therefore, the transductance of the JFET is given by,

$$g_m = \left.\frac{\Delta i_D}{\Delta v_{GS}}\right|_{V_{GS}=\text{constant}} = 7.5\ m\Omega^{-1}$$

Design of JFET amplifier:

To design a JFET amplifier, the Q point for the dc bias current can be determined graphically. The dc bias current at the Q point should lie between 30% and 70% of I_{DSS}. This locates the Q point in the linear region of the characteristic curves.

The relationship between i_D and v_{GS} can be plotted on a dimensionless graph (i.e., a normalized curve) as shown in **fig. 2** .

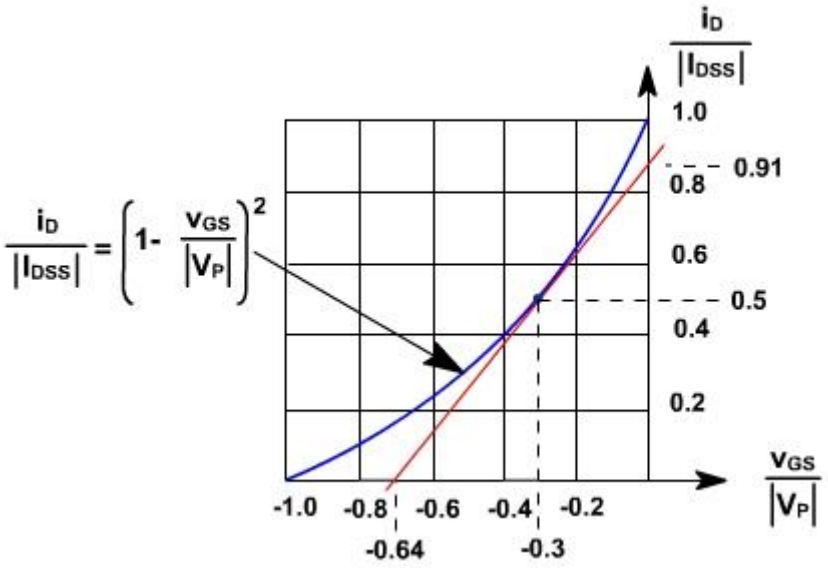


Fig. 2

The vertical axis of this graph is i_D / I_{DSS} and the horizontal axis is v_{GS} / V_P. The slope of the curve is g_m.

A reasonable procedure for locating the quiescent point near the center of the linear operating region is to select $I_{DQ} \approx I_{DSS} / 2$ and $V_{GSQ} \approx 0.3V_P$. Note that this is near the midpoint of the curve. Next we select $v_{DS} \approx V_{DD} / 2$. This gives a wide range of values for v_{ds} that keep the transistor in the pinch ?off mode.

The transductance at the Q-point can be found from the slope of the curve of **fig.2** and is given by

$$g_m = \frac{1.41\ I_{DSS}}{V_P}$$

Example-2

Determine g m for a JFET where I_{DSS} = 7 mA, V_P = -3.5 V and V_{DD} = 15V. Choose a reasonable location for the Q-point.

Solution:

Let us select the Q-point as given below:

$$I_{DQ} = \frac{I_{DSS}}{2} = 3.5 \text{ mA}$$

$$V_{DSQ} = \frac{V_{DD}}{2} = 7.5 \text{ V}$$

$$V_{GSQ} = 0.3V_P = -1.05 \text{V}$$

The transconductance, g_m, is found from the slope of the curve at the point $i_D / I_{DSS} = 0.5$ and $v_{GS} / V_P = 0.3$. Hence,

$$g_m = \frac{1.41\ I_{DSS}}{V_P} = 2840\ \mu\Omega^{-1}$$

JEFT as Analog Switch:

JFET can be used as an analog switch as shown in **fig. 3**. It is the major application of a JFET. The idea is to use two points on the load line: cut off and saturation. When JFET is cut off, it is like an open switch. When it is saturated, it is like a closed switch.

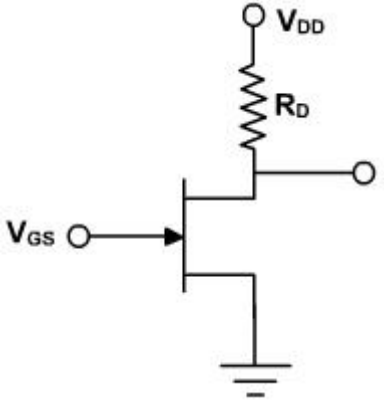


Fig. 3

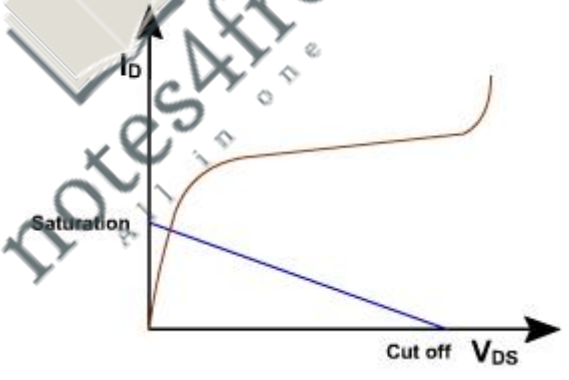


Fig. 4

When $V_{GS} = 0$, the JFET is saturated and operates at the upper end of the load line. When V_{GS} is equal to or more negative than $V_{GS}(off)$, it is cut off and operates at lower end of the load line (open and closed switch).This is shown in **fig. 4**.

Only these two points are used for operation when used as a switch. The JFET is normally saturated well below the knee of the drain curve. For this reason the drain current is much smaller than I_{DSS} .

FET as a Shunt Switch:

FET can be used as a shunt switch as shown in **fig. 5**. When V_{cont}=0, the JFT is saturated and the switch is closed When V_{cont} is more negative FET is like an open switch. The equivalent circuit is also shown in **fig. 5**.

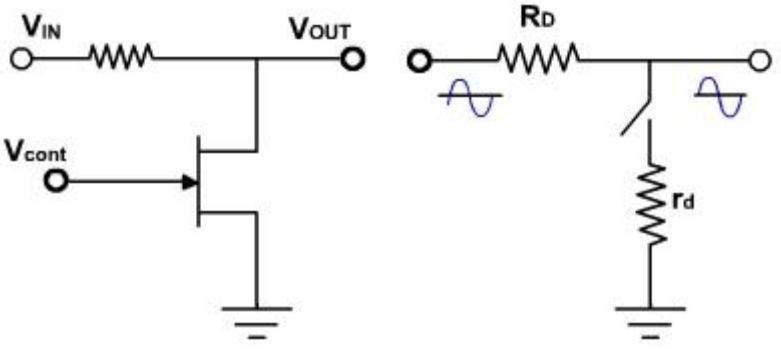


Fig. 5

FET as a series switch:

JFET can also be used as series switch as shown in **fig. 6**. When control is zero, the FET is a closed switch. When V_{con}= negative, the FET is an open switch. It is better than shunt switch.

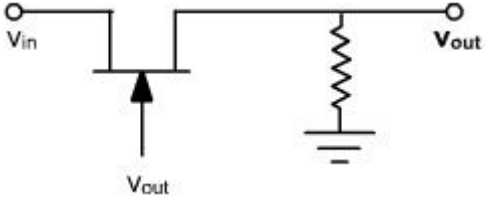


Fig. 6

Multiplexing:

One of the important application of FET is in analog multiplexer. Analog multiplexer is a circuit that selects one of the output lines as shown in **fig. 7**. When control voltages are more negative all switches are open and output is zero. When any control voltage becomes zero the input is transmitted to the output.

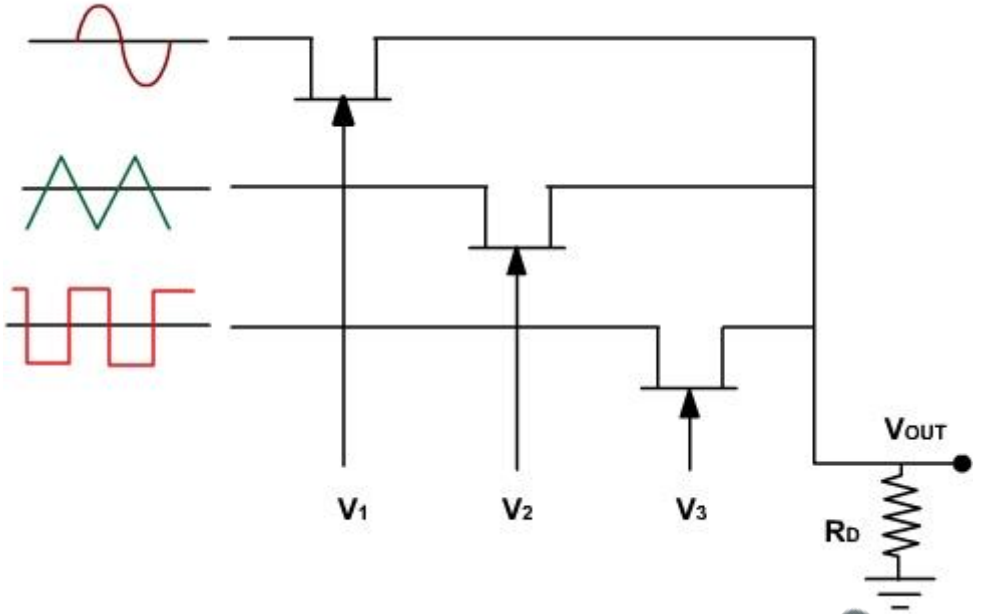


Fig. 7